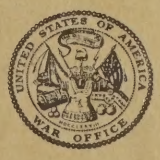
TM 11-5895-312-30

DEPARTMENT OF THE ARMY TECHNICAL MANUAL

DS MAINTENANCE MANUAL

RECEIVER-TRANSMITTER DIGITAL DATA R-1251/MSQ



HEADQUARTERS, DEPARTMENT OF THE ARMY
JANUARY 1965

WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working on dc power supply circuits or on ac line connections.

DON'T TAKE CHANCES!

EXTREMELY DANGEROUS VOLTAGES EXIST IN ALL CONSOLE UNITS

TECHNICAL MANUAL
No. 11-5895-312-30

HEADQUARTERS
DEPARTMENT OF THE ARMY
WASHINGTON, D.C., *8 January 1965*

DS Maintenance Manual

RECEIVER-TRANSMITTER, DIGITAL DATA R-1251/MSQ

*This manual supersedes TM 11-5895-312-30, 9 August 1963.

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1. Scope

a. This manual contains direct support maintenance information for Receiver-Transmitter, Digital Data R-1251/MSQ (transmitter-receiver), part of Weapons Monitoring Center OA-4342/MSQ-28B or OA-4972/MSQ-56 (WMC) and Processing Center, Radar Data OA-4333/MSQ-28B (RDPC). The WMC and RDPC are part of Antiaircraft Defense System AN/MSG-4 (AN/MSG-4 System). Maintenance information in this manual consists of functioning, troubleshooting, removal and replacement, alignment and adjustment, references (app.), and a glossary. The illustrations support the text, and the troubleshooting charts reference unit and card assemblies within the transmitter-receiver.

b. One transmitter-receiver (502602) is included in the RDPC and three transmitter-receivers are included in the WMC. For details on how the transmitter-receiver functions in the AN/MSG-4 System, and for procedures to sectionalize troubles to the transmitter-receiver, refer to TM 11-5840-271-30/18 (RDPC) or TM 11-5840-272-30/17 (WMC) subsystem maintenance information volumes, as applicable.

2. Index of Publications

Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment. DA Pam 310-4 is an index of current technical manuals, technical bulletins, supply manuals, supply catalogs supply bulletins, lubrication orders, and modification work orders that are available through publications supply channels. The index lists the individual parts (-10, -20, -35P, etc.) and the latest changes to and revisions of each equipment publication.

3. Forms and Records

a. Reports of Maintenance and Unsatisfactory Equipment. Use equipment forms and records in accordance with instructions in TM 38-750.

b. Report of Damaged or Improper Shipment. Fill out and forward DD Form 6 (Report of Damaged or Improper Shipment) as prescribed in AR 700-58 (Army), NAVSANDA Publication 378 (Navy), and AFR 71-4 (Air Force).

c. Reporting of Equipment Manual Improvements. The direct reporting, by the individual user, of errors, omissions, and recommendations for improving this manual is authorized and encouraged. DA Form 2028 (Recommended Changes to DA Publications) will be used for reporting these improvements. This form will be completed in triplicate by the use of pencil, pen, or typewriter. The original and one copy will be forwarded direct to Commanding General, U.S. Army Electronics Command, ATTN: AMSEL-MR-MA, Fort Monmouth, N.J., 07703. One information copy will be furnished to the individual's immediate supervisor (officer, noncommissioned officer, supervisor, etc.).

4. General Information

a. Graphic symbols used on the illustrations are in accordance with those listed in 1 MIL STD-17.

b. Components mentioned frequently in this manual are usually referred to by common name.

c. Assembly numbers used on drawings refer to the manufacturer's part numbers.

d. Equipment panel markings are capitalized in text and are blocked on illustrations.

e. Broken lines on illustrations represent mechanical connections, solid lines indicate electrical connections, and heavy solid lines inclose circuit groups within the function.

f. The use of this manual requires a basic knowledge of transistors as contained in TM 11-690 and digital fundamentals as contained in TM 11-5895-264-25.

g. Abbreviations and definitions of unusual terms used in this manual are contained in the glossary.

h. The unit schematic diagram for the transmitter-receiver is contained in this manual.

i. The card assembly schematic diagrams for the transmitter-receiver are contained in this manual.

j. The unit schematic diagrams for the power supplies and power control panels are contained in TM 11-5840-273-30.

Section II. DESCRIPTION AND DATA

5. Purpose and Use

The transmitter-receiver provides a digital communication capability between subsystems of the AN/MSG-4 System. Each transmitter accepts data in the form of digital signals from output buffers and converts these data into modulated signals, either frequency shift modulated (FSM) or pulse code modulated (PCM), for transmission between subsystems. Each receiver accepts the modulated signals (FSM or PCM) and reconverts them into data that are supplied to input buffers. A total of four transmitter-receivers are used in the AN/MSG-4 System, three of which are in the WMC and the fourth is in the RDPC.

6. Technical Characteristics

Dc voltage requirements.	+300 volts dc ±3 volts.
	+150 volts dc ±1.5 volts.
	+50 volts dc ±5 volts.
	+28 volts dc ±2.8 volts.
	+1.5 volts dc ±0.02 volt.
	−6 volts dc ±0.06 volt.
	−7.5 volts dc ±0.08 volt.
	−28 volts dc ±2.8 volts.
	−50 volts dc ±5 volts.
	−26.5 volts dc ±0.27 volt.
Ac voltage requirements.	120 volts ac, 400 cps ±5 volts.
Line frequencies	600, 1,125, 1,500, and 1,875 cps.
Pulse rate	750 pps.

7. Components

Each transmitter-receiver is functionally divided, for discussion purposes, into three circuit areas referred to as subfunctions: a transmitter subfunction, a receiver subfunction, and a power supply subfunction. The following lists the components contained in each subfunction.

a. Transmitter Subfunction.

Manufacturer's No.	Components	Quantity
549591	600-cps oscillator and modulator.	1
1518471	Modulator gate and oscillator	1
1518484	Modulator output	1
1518493	6-kc and 750-pps CP generator	1
1518494	Frequency divider	2
1522312	Variable gain amplifier and transmitter relay card.	1

b. Receiver Subfunction.

Manufacturer's No.	Components	Quantity
1518324	Data input filter and first limiter amplifier.	2
1518326	Second limiter amplifier and frequency discriminator.	2
1518327	Data logic amplifier	2
1518325	1,500-cps detector	2
1593982	IRP and DCP generator	2
1518302	Synchronizer No. 1	2
1518303	Synchronizer No. 2	2
1522307	Receiver relay card	2
1518428	Amplifier demodulator chassis	2
1518486	Slicer	2
1522348	Detector start/remote	2

c. Power Supply Subfunction.

Manufacturer's No.	Components	Quantity
547885	Filter card	1
1512530	±12-volt power supply	1
1512552	−12-volt regulator and protection circuit.	1

8. Description and Location of Equipment

a. Description. A complete description of the components of the transmitter-receiver and illustrations showing the location of the transmitter-receivers in the RDPC and WMC are given in TM 11-5840-271-30/1 and TM 11-5840-272-30/1.

b. Location. The RDPC and WMC transmitter-receivers are located as follows:

(1) *RDPC.* The RDPC contains one transmitter-receiver in one drawer. The unit has reference designator 51 and is contained in group No. 91.

(2) *WMC.* The WMC contains three transmitter-receivers in three drawers. The unit locations are as follows:

Unit	Unit No.	Reference designator	Group No.
Transmitter-receiver 1	502602	48	78
Transmitter-receiver 2	502602	49	79
Transmitter-receiver 3	502602	50	80

9. Additional Equipment Required

The transmitter-receiver depends on associated equipment for power. Most filtered and regulated operating voltages are obtained from power supplies in the RDPC or WMC. The transmitter-receiver power supply subfunction performs additional filtering and regulating for some of these voltages.

10. Message Composition

The transmission of message data between the RDPC, WMC, and remote sites is accomplished by the use of serial binary signals. These messages may be either FSM or PCM. Each true digit in a PCM message is signified by 2 cycles of a 1,500-cycle-per-second (cps) signal, and each false digit is signified by the absence of the 1,500-cps signal. Each true digit in an FSM message is signified by the presence of a 1,125-cps signal, and each false digit is signified by the presence of a 1,875-cps signal. For message synchronization, the beginning of an FSM message contains 1,500-cps signals which are a part of the ready start word (*a* below), and the beginning of the PCM message contains 600-cps signals mixed with 1,500-cps signals in the ready start word (*b* below). The format of the various messages processed by the transmitter-receiver is described in TM 11-5840-271-30/1 and TM 11-5840-272-30/1.

a. FSM Ready Start Word. The FSM ready start word consists of four time slots (1.33-millisecond periods) of 1,500-cps (midfrequency) signals. The midfrequency is present during time slots 00, 0, 1, and 2. The FSM message contains 83 time slots which are numbered 00 through 81.

b. PCM Ready Start Word. The PCM ready start word consists of three time slots of 600-cps signals mixed with 1,500-cps signals. The mixed frequencies are present during time slot 0 through time slot 2. The PCM message contains 82 time slots which are 0 through 81.

c. FSM Remote Start Word. The FSM remote start word consists of four time slots of 1,500-cps signal which is transmitted by the BN/BTRY ADL sequencer function (TM 11-5840-272-30/9). The remote start word is received only by the transmitter-receiver used in the self-test function of the WMC (TM 11-5840-272-30/16).

CHAPTER 2

GENERAL FUNCTIONAL ANALYSIS

11. Introduction

Each transmitter-receiver consists of one transmitter and two separate receivers. The WMC contains three transmitter-receivers, which comprise three transmitters and six receivers. The RDPC contains one transmitter-receiver which comprises one transmitter and two receivers. Transmitter and receiver signal routing is described in *a* and *b* below. Each transmitter and each receiver is a part of a function in either the WMC or the RDPC. Transmitter and receiver functional usage is shown in the following chart:

Transmitter or receiver	Part of—	Subsystem volume
WMC receivers 1A, 1B, 2A, and 2B.	Remote input buffers function	TM 11-5840-272-30/3
WMC receiver 3A	Local input buffer and data controls function.	TM 11-5840-272-30/2
WMC receiver 3B	Self-test function	TM 11-5840-272-30/16
RDPC receivers 1A and 1B	Data exchange function (one receiver is spare).	TM 11-5840-271-30/2
WMC transmitter 1	Remote output buffer function	TM 11-5840-272-30/14
WMC transmitter 2	Local output buffer function	TM 11-5840-272-30/13
WMC transmitter 3	Self-test function	TM 11-5840-272-30/16
RDPC transmitter 1	Data exchange function	TM 11-5840-271-30/2

a. Transmitters.

(1) *RDPC transmitter* (fig. 1). Output buffer 501054 supplies data control and ready control signals to the transmitter. These signals are synchronized in the output buffer by 750-pulses-per-second (pps) transmitter (T)-pulses supplied by the transmitter. The modulated message (message frame) is transmitted to the WMC through telephone test set 501896 and communication test panel 501074, both of which are in communications central 501165.

(2) *WMC transmitter 1* (fig. 2). Data control and ready control signals are supplied to transmitter 1 through communications test panel 502074 in communications central 502165 from remote output buffer 502146. The 750-pps T-pulses are routed from the transmitter to the output buffer via the 502074. The modulated message is transmitted through telephone test set 501896, telephone relay rack 502138, and the 502074 (all in communications central 502165) to remote stations.

(3) *WMC transmitter 2* (fig. 3). Local output buffer 502047 supplies the data control and ready control signals to, and receives 750-pps T-pulses from, transmitter 2 through the 502074. The modulated message is transmitted through the 502138 and the 502074 to the RDPC.

(4) *WMC transmitter 3* (fig. 4). Transmitter 3 is used with the central control indicator (CCI). Test information set in

manually (on ADL test set panel 502054) controls the output of central control indicator 1, 502044 to transmitter 3 through the 502074. The modulated message is routed to the 502138 and the 502074 where it may be used by patching it to other jacks on the 502074.

b. Receivers.

(1) *RDPC receivers* (fig. 1). The RDPC receiver A or B message (normally from the WMC) is routed through communications test panel 501074 and input buffer 501053 to the receivers. The receiver outputs are routed back to the 501053.

(2) *WMC receivers 1A, 1B, 2A, and 2B* (figs. 2 and 3). Receiver A and B messages from the remote stations are routed through communications test panel 502074 to the four receivers. The receiver outputs are routed to remote input buffers 1–4 (502027). Receiver 1A is associated with remote station 3 and remote input buffer 3, 1B with remote station 4 and remote input buffer 4, 2A with remote station 1 and remote input buffer 1, and 2B with remote station 2 and remote input buffer 2.

(3) *WMC receiver 3A* (fig. 4). Local data from the RDPC (receiver A message) are routed through communications test panel 502074 to receiver 3A. Outputs from receiver 3A are supplied to local input buffer 502046.

(4) *WMC receiver 3B* (fig. 4). Display information (CCI inputs), is patched into the 502074 as test information for CCI display and routed through central control indicator 2 (502049) to receiver 3B as receiver B message. (See TM 11-5840-272-30/16.) Receiver 3B outputs are routed through the 502044 to the 502054 and 502049 for display at the ADL test set panel.

12. Functional Description

(fig. 5)

Since all of the transmitter-receiver circuits are identical, only one transmitter-receiver is described in this manual. For description, the transmitter-receiver is divided into a transmitter subfunction, a receiver subfunction, and a power supply subfunction. Since both receivers operate identically, only one is described.

13. Transmitter Subfunction

(fig. 7)

The transmitter subfunction receives data and ready control signals. The data signal is a series of digital bits which pertain to track information. The ready signal is a digital signal which signifies the start of a message. The transmitter subfunction processes the data and ready signals to generate PCM or FSM messages, depending on the type of transmission required. For FSM message transmissions, each true bit is signified by a 1,125-cps signal (mark frequency), and each false bit is signified by a 1,875-cps signal (space frequency). These two frequencies are 375 cps on opposite sides of a 1,500-cps midfrequency. For PCM message transmissions, each true bit is signified by a pulse modulated by 2 cycles of a 1,500-cps signal and each false bit is signified by the absence of a signal. Each message begins with a sync word that is part of the modulated message output. The sync word is generated as a result of processing the ready signal. The FSM sync word contains four bits of the midfrequency, three bits of the mark frequency, one bit of the space frequency, and one bit of the mark frequency. The sync word transmitted for PCM messages contains six bits of 1,500 cps mixed with 3 bits of 600 cps, one blank bit (no signal present) and a final bit of 1,500 cps. (See TM 11-5840-271-30/1 and TM 11-5840-272-30/1 for a graphic representation.) Because the data signal and the various transmitting frequencies must be synchronized, 750-pps transmitter (T)-pulses are generated in the transmitter and supplied to the data source for synchronization purposes. A 6-kilocycle (kc) square wave signal is generated in the FSM modulator circuits, regardless of operating mode, and routed to the receiver subfunction synchronizer circuits to generate a 6-thousand-pulses-per-second (kpps) clock pulse.

14. Receiver Subfunction

(fig. 6)

Each receiver subfunction receives modulated messages (either FSM or PCM) from a transmitter, demodulates and synchronizes the received messages, and supplies synchronized data, input ready pulse, and delayed clock pulses to the

RDPC or WMC functional area requiring this information. Since two methods of modulation exist (FSM or PCM), separate circuits in the receiver are used to demodulate each type of received message. Before data are routed to the synchronizer circuits, $\overline{\text{ready}}$ (for PCM messages) or $\overline{\text{ready}}$ $\overline{\text{start}}$ (for FSM messages) resets a counter and flip-flops in the synchronizer circuits. The synchronizer circuits retime the data and generate an input ready pulse (IRP) each time a message is received. The IRP is used to signify that a valid message is to follow. The synchronizer circuits also generate delayed clock pulses that synchronize a time slot counter, in the associated functional area, with data from the receiver. The input ready pulse and delayed clock pulses are generated by use of a 6-kc square wave signal received from the transmitter subfunction.

15. Power Supply Subfunction

(fig. 5)

The power supply subfunction contains a ± 12-volt regulated power supply. This subfunction also filters and regulates other voltages, and supplies filtered, regulated, and unregulated direct current (dc) voltages to the transmitter-receiver.

CHAPTER 3

RECEIVER SUBFUNCTION, DETAILED FUNCTIONAL ANALYSIS

Section I. PCM DEMODULATOR CIRCUITS

16. General

(fig. 37)

The PCM demodulator circuits for receivers A and B are identical; therefore, only receiver A circuits are described in detail. The PCM demodulator circuits accept the PCM message from the receiver relay card in the form of 1,500-cps sine waves at a 750-bit rate. Included at the beginning of the message, as a part of the sync word, is the 600-cps ready signal. The 600-cps ready signal and 1,500-cps data are amplified and separated (demodulated) and then filtered to become the smoothed ready and smoothed data signals. The smoothed ready and data signals are then routed through a slicer assembly where 0-volt and 12-volt logic levels, representing the signal and its logical complement, are formed. The sliced data and ready signals and their complements are then routed to the receiver synchronizer circuits for synchronization.

17. Receiver Relay Card

(fig. 37)

The receiver message is applied to contacts 2, 6 of relay K1 on 1522307, J20B (receiver A) and of J19C (receiver B). Relay K1 is controlled by receiver FSM-PCM select switch S1. When PCM messages are being demodulated, S1 is set to the PCM position and K1 is energized. The PCM message is routed through closed contacts 2–5, and 6–1 to amplifier demodulator chassis 1518428, J2B–J9B (receiver A) or J1C–J8C (receiver B).

18. Amplifier Demodulator Chassis

(fig. 37)

The PCM message is routed through input transformer T1, high-pass filter FL1, and MESSAGE LEVEL adjust R1 to automatic gain control (agc) amplifier V1. Transformer T1 is an impedance-matching and step-up transformer. Filter FL1 removes noise below 200 cps. MESSAGE LEVEL adjust R1 adjusts the level of the signal at the input to V1. The gain of agc amplifier V1 is controlled by a feedback network from CR1–CR4 or a fixed bias provided by R14 and R15. The output of V1 is amplified by V2A and routed to separation filter FL2. Filter FL2 separates the 1,500-cps and 600-cps signals, and applies these signals to a pair of full-wave bridge rectifiers. The output of each rectifier is applied to low-pass filter FL3 where the ripple is reduced. The filter output approximates a square wave signal for each data bit (1,500-cps input) or ready bit (600-cps input). These signals are routed to a slicer assembly as smoothed data and smoothed ready signals. The rectified 1,500-cps signal from full-wave bridge rectifier CR1–CR4 is also routed to feedback amplifier V2B. Amplifier V2B controls the gain of agc amplifier V1 when AGC–DISABLE switch S1 is in the AGC position. The gain provided by V2B is controlled by AGC adjust R12. The V2B output can never be more positive than −4 volts because of −4-volt clamp CR9. The feedback signal from V2B is rectified by CR10 and routed through AGC–DISABLE switch S1, filtered by C7 and R16 and applied to V1. Any change in the amplitude of the rectified 1,500-cps signal from bridge rectifier CR1–CR4 is fed back through V2B; this action causes the gain of V1 to be changed proportionately and thus automatically keeps the amplifier demodulator chassis output constant. When AGC–DISABLE switch S1 is placed in the DISABLE position, −11 volts from voltage divider R14, R15 is applied to V1 as a fixed bias, and V1 acts like a low gain amplifier.

19. Data and Ready Slicer Circuits

(fig. 37)

The data and ready slicer circuits shape the smoothed ready and smoothed data signals, and also generate the logical complement of these

signals. The ready and data slicer circuits function identically; therefore, only the data slicer circuit is explained. The ready slicer circuit reference designators differ; the difference is shown in figure 37. The data slicer circuit consists of slicer adjust R4, amplifier Q1, Schmitt trigger shaper Q2, Q3, emitter followers Q4 and Q6, and inverters Q5 and Q7.

a. Amplifier Q1. The smoothed data signal from the amplifier demodulator is applied to amplifier Q1 in the slicer. Transistor Q1 is a temperature-stabilized, variable-gain amplifier that controls the pulse width output of Schmitt trigger shaper Q2, Q3. Triggering of the Schmitt trigger shaper is controlled by the amplitude of the Q1 output. Slicer adjust R4 controls the amplitude of the Q1 output by changing its biasing voltage. Slicer adjust R4 is adjusted so that the output of the slicer is one time slot (1.33 millisecond) wide.

b. Schmitt Trigger Shaper Q2, Q3. A Schmitt trigger shaper is a bistable device that changes states with a change in the amplitude of the input signal. The amplitude of the signal from Q1 determines when Q2 is conducting or nonconducting. Transistor Q3 is always in the opposite state of conduction from Q2. A negative pulse (smoothed data) applied to Q1 causes Q2 to conduct and Q3 to cut off. When the smoothed data signal is not present, Q2 is cut off and Q3 is conducting. Thus, the outputs are logical complements of each other. The Q3 output is applied to emitter follower Q4, and the Q2 output is applied to emitter follower Q6.

c. Emitter Follower Q6 and Inverter Q7. The output is current-amplified by Q6 and inverted by Q7. The Q7 output is routed to the synchronizer circuits as the data PCM receiver (A) signal.

d. Emitter Follower Q4 and Inverter Q5. The Q3 output is current-amplified by Q4 and inverted by Q5. The Q5 output is routed to the synchronizer circuits as $\overline{\text{data}}$ PCM receiver (A).

e. Data and Ready Routing for Receiver 3B. Data, ready, $\overline{\text{data}}$, and $\overline{\text{ready}}$ from receiver 3B are routed to the self-test function and to the synchronizer circuits. The signals fed to the self-test function are used for test purposes only.

Section II. FSM DEMODULATOR CIRCUITS

20. General

The FSM demodulator circuits accept the FSM message from the receiver relay card in bit intervals (time slots) of 1,125-cps, 1,500-cps, and 1,875-cps signals at a 750-bit-per-second (bps) rate. The signals are amplified, filtered, and limited. Filtering removes any noise above or below the signal frequencies. The limiting amplifier clips signal peaks that exceed ± 3.1 volts. After being limited, the signal frequencies are separated in detector circuits and the resulting signals are routed to the synchronizing circuits as FSM data and ready start signals. The circuits for receivers A and B are identical; therefore, only receiver A circuits are described in detail.

21. Receiver Relay Card

(fig. 38①)

The receiver A message is applied to receiver relay K1 on 1522307, J20B (J19C for receiver B). Receiver FSM–PCM select switch S1 controls relay K1. When S1 is set to the FSM position, K1 is deenergized, and the FSM receiver message is routed through closed contacts 2–4 and 6–8 to the data input filter and first limiter amplifier.

22. Data Input Filter and First Limiter Amplifier

(fig. 38①)

The data input filter and first limiter amplifier provides isolation, amplification, and bandpass limiting in two circuits as follows:

a. Data Input Circuit. The data input circuit consists of an input transformer, isolation pad, voltage limiter, and a bandpass filter. The FSM message is applied to input transformer T1, which couples the incoming message to bandpass filter FL1 through isolation pad R1, R2, R3, and voltage limiter CR1, CR2. The isolation pad is an impedance-matching network that matches the 600-ohm transformer to the voltage limiter and isolates the voltage limiter and all circuits which follow from the input line. The voltage limiter limits the signal into the bandpass filter to a maximum level of ± 12 volts. Bandpass filter FL1 filters out all frequencies above and below the signal frequencies. The output of FL1 is applied to the first limiter amplifier circuit.

b. First Limiter Amplifier Circuit. The first limiter amplifier circuit consists of differential amplifier Q1, Q2, emitter followers Q3 and Q5, inverter Q4, and a feedback loop that includes feedback limiters Q6 and Q7. The FSM message from FL1 is applied to differential amplifier Q1, Q2. Feedback limiter Q6, Q7 controls the input level of the differential amplifier and therefore the output of the first limiter amplifier circuit. Differential amplifier Q1, Q2 output is current-amplified by emitter follower Q3, inverted by inverter Q4, and routed through emitter follower Q5 to the second limiter amplifier and frequency discriminator as filtered data (FSM). Emitter follower Q5 provides isolation between the first and second limiter amplifiers. Because of the feedback loop provided from Q5 output through Q6 and Q7 to Q1 and Q2, the amplifier output signal at TP2 does not exceed ±3.1 volts.

23. Second Limiter Amplifier and Frequency Discriminator

(fig. 38①)

Second limiter amplifier and frequency discriminator 1518326, J13B–J14B for receiver A (J12C–J13C for receiver B) consists of the second limiter amplifier circuit, squaring amplifier circuit, and part of the frequency discriminator circuit. Data logic amplifier 1518327, J15B–J16B for receiver A (J14C–J15C for receiver B) also contains a portion of the frequency discriminator circuit.

a. Second Limiter Amplifier Circuit. The second limiter amplifier circuit operation is identical with the first limiter amplifier (para. 22*b*). The circuit consists of differential amplifier Q6, Q7, emitter followers Q8 and Q10, inverter Q9, and feedback limiters Q4, Q5. The second limiter amplifier insures that the amplitude of the data signal applied to the squaring amplifier is ±3.5 volts.

b. Squaring Amplifier Circuit. The output of the second limiter amplifier circuit is applied to saturation amplifier Q1, amplified and applied to saturation amplifier Q2. The Q2 output is applied to emitter follower Q3. Feedback from Q2 and Q3 is in phase with the input of Q1, causing regeneration and, therefore, the squaring action. The Q3 output is a series of square waves (fig. 8) that are routed to the frequency discriminator circuit to trigger the one-shot multivibrators.

c. Frequency Discriminator Circuit. The frequency discriminator circuit consists of one-shot multivibrators Q11, Q12, Q13, and Q14, Q15, Q16, and negative or gate Q17, CR6, CR11, R48 on 1518326, and also resistor-diode isolation network CR1–CR4 and low-pass filter FL1 on 1518327. The square wave signals from the squaring amplifier trigger the one-shot multivibrators. Multivibrator Q11, Q12, Q13 is triggered by the negative-going portion of the square wave signal, and multivibrator Q14, Q15, Q16 is triggered by the positive-going portion of the square wave signal. The outputs of the multivibrators are applied to negative or gate Q17, CR6, CR11, R48. The or gate output is a series of positive pulses (fig. 8) that are applied to resistor-diode isolation network CR1–CR4 on the 1518327. The data signal is changed by the resistor-diode isolation network and filter from a series of positive pulses to voltages proportional to the input signal frequency. Filter FL1 also reduces the ripple component to provide voltage levels proportional to the signal frequencies as follows: midfrequency, approximately 0 volt; mark frequency, approximately +3.5 volts; and space frequency, approximately −10 volts (fig. 8). The output of FL1 is applied, in combination with the output of voltage level control R6, to differential amplifier Q1, Q2 in the base-band data limiter amplifier circuit.

24. Base-Band Data Limiter Amplifier Circuit

(fig. 38①)

The base-band data limiter amplifier circuit is located on assembly 1518327, J15B–J16B for receiver A (J14C–J15C for receiver B), and consists of voltage level control R6, differential amplifier Q1, Q2, emitter followers Q3 and Q5, inverter Q4, and feedback limiters Q6, Q7. Low-pass filter FL1 output from the frequency discriminator circuit is applied to differential amplifier Q1, Q2. Voltage level control R6 is adjusted so that the output from the base-band data limiter amplifier circuit is 0 volt when the midfrequency is present at the input of the discriminator circuit. The differential amplifier output is current-amplified by emitter follower Q3 and routed through inverter Q4 to emitter follower Q5. The output of Q5 is routed through feedback limiters Q6, Q7 to the input of differential amplifier Q1, Q2. Feedback limiters Q6, Q7 limit the signal into Q1, Q2 so that the output at Q5 has a

maximum and minimum level of ±7.5 volts. The voltage level of +3 volts or greater corresponds to a space frequency (1,875 cps) in the incoming FMS message, and a voltage of −3 volts or less corresponds to a mark frequency (1,125 cps) in the incoming FSM message. The midfrequency (1,500 cps) is represented at this point by 0 volt. The output of the base-band data limiter amplifier circuit (BBD illustrated on fig. 8) is applied to a data detector circuit and to 1,500-cps detector 1518325, J17B–J18B for receiver A (J16C–J17C for receiver B).

25. Data Detector Circuit

(fig. 38①)

The data detector circuit, located on assembly 1518327 (J15B–J16B, receiver A and J14C–J15C, receiver B), consists of a differential amplifier (Q8, Q9), emitter follower Q10, inverter Q11, and switches Q12 and Q13. The data detector circuit converts the BBD signal to logic level data and $\overline{\text{data}}$ signals. When BBD is more positive than 0 volt (false data bit in the FSM message), the output of differential amplifier Q8, Q9 goes to 0 volt. The differential amplifier output is routed through emitter follower Q10 to switch Q13 and to inverter Q11. A 0-volt input to Q10 causes the output of Q13 (data) to be approximately −12 volts. The 0-volt input to Q10 causes the Q11 output to be −12 volts which is routed to switch Q12. The −12-volt input to switch Q12 causes the output of Q12 ($\overline{\text{data}}$) to be 0 volt. When BBD is more negative than 0 volt (true data bit in the FSM message), the differential amplifier output is approximately −12 volts. This potential causes the output of Q12 ($\overline{\text{data}}$) to be −6 volts and the output of Q13 (data) to be 0 volt. Data and $\overline{\text{data}}$ are routed to the synchronizer circuits.

26. Detector, 1,500-Cps

(fig. 38②)

The 1,500-cps detector (1518325) consists of three detectors: mark detector, space detector, and MFC detector.

a. Mark Detector. Mark detector flip-flop Q1, Q2, detects a −3-volt level (mark frequency present) in the BBD input from data logic amplifier 1518327. The mark detector flip-flop output is 0 volt when BBD is −3 volts or greater, and is −10 volts when the BBD signal is either 0 volt (midfrequency present) or +3 volts, or greater (space frequency present). The mark detector flip-flop output is routed to inverter Q13. The Q13 output is coupled to MFC nor gate Q3 and to detector start/remote 1522348 as the −3-volt detector signal.

b. Space Detector. Space detector flip-flop Q9, Q10, detects a +3-volt level (space frequency) in the BBD input. The space detector flip-flop output is 0 volt when BBD is +3 volts, and −10 volts when the BBD signal is either 0 volt (midfrequency present) or −3 volts (mark frequency present). The space detector flip-flop output is routed through inverter Q8 to MFC nor gate Q3, and to detector start/remote 1522348 as the +3-volt detector signal.

c. MFC Detector. The MFC (midfrequency control) detector consists of nor gate Q3, low-pass filter FL1, a differential amplifier (Q11, Q12), switches Q4–Q6, inverter Q7, and balance control R33. When the BBD signal is ±3 volts or greater (mark or space frequency present), the outputs of inverter Q13 and Q8 are complementary and the MFC nor gate output is at 0 volt. When BBD is 0 volt (midfrequency present), the outputs of Q13 and Q8 are both 0 volt, and the MFC nor gate output is negative. The midfrequency component of a message is present during the first four time slots in the sync word of an incoming message; therefore, the output of the nor gate is a negative 5.32-millisecond pulse. The output of the nor gate is coupled to low-pass filter FL1 which delays the 5.32-millisecond pulse and rounds the leading and trailing edges of the pulse. The output of FL1 is amplified by differential amplifier Q11, Q12. The differential amplifier output is fed to switch Q4, Q5 which operates together with MFC switch Q6 to decrease the risetime and falltime of the differential amplifier output signal. The voltage level of the output of Q11, Q12 controls switch Q4, Q5. The output of switch Q4, Q5 controls the turn-on and turn-off of MFC switch Q6. Balance control R33 controls the width of the output pulse at switch Q6 by varying the gain of the differential amplifier. The output of Q6 is coupled to inverter Q7, and also routed as MFC to detector start/remote 1522348. The output of Q7 is routed as $\overline{\text{MFC}}$ to the same assembly.

27. Detector Start/Remote

(fig. 38②)

Detector start/remote 1522348 is located in J19B for receiver A and J18C for receiver B. It consists of a ready start detector circuit and a remote start detector circuit.

a. Ready Start Detector Circuit (fig. 8). The ready start signal is generated when a sync word (para. 10) is detected in an incoming FSM message. The ready start circuit consists of MFC one-shot multivibrator Q1, Q2, inverter Q3, MFC clamp Q6, Q7, Q8, logic converter Q9, integrator Q10, integrator reset Q15, ready start switch Q11, and negative and gate Q4. The MFC one-shot multivibrator is turned on by the negative-going edge of the MFC signal, causing the output to go to −10 volts. The −10-volt signal is routed through inverter Q3 to and gate Q4. The output of Q3 is 0 volt when the MFC one-shot multivibrator output is −10 volts. The $\overline{\text{MFC}}$ signal is applied to integrator reset Q15. The integrator reset circuit differentiates the negative-going edge of the $\overline{\text{MFC}}$ signal and generates a positive pulse that resets the Q10 output to +12 volts. The −3-volt detector signal is applied to logic converter Q9, where it is inverted and applied to Q10. When the −3-volt detector signal goes negative at the start of time slot 3 (fig. 9), the integrator output decreases at an exponential rate from +12 volts to 0 volt. When the integrator output reaches 0 volt, approximately 3 milliseconds after the −3-volt detector signal goes negative, the output of ready start switch Q11 goes from −12 volts to 0 volt. The Q11 output is applied to and gate Q4, With both inputs to Q4 at 0 volt, the output of Q4 (ready start) goes to −12 volts. Ready start is routed to the synchronizer circuits where it is detected by F/FSQ5 (para. 32). The SQ5 signal is routed from the synchronizer circuit to the or gate associated with MFC clamp Q6, Q7, Q8. When signal SQ5 goes to 0 volt, the output of the MFC clamp goes to 0 volt, clamping the output of the MFC one-shot multivibrator to 0 volt. The multivibrator output at 0 volt causes the output of Q3 to go to −10 volts and the output of Q4 (ready start) to go to 0 volt (fig. 10). Signal SQ4 from the synchronizer circuits is also applied to the or gate associated with the MFC clamp. The SQ4 signal prevents erroneous ready start signals from being generated by clamping the MFC one-shot multivibrator to 0 volt when signal SQ4 is 0 volt (para. 32). The remaining input to the MFC or gate is discussed in *b* below.

b. Remote Start Detector Circuit (fig. 8). The remote start detector circuit is used only by receiver B of transmitter-receiver 3 which is associated with the self-test function (TM 11-5840-272-30/16). The remote start signal is used to synchronize circuits in the self-test function for display of BN/BTRY ADL messages on the automatic data link (ADL) test set panel. The remote start detector circuit detects any FSM remote start signal (para. 10) that is received by the FSM demodulator circuits. The demodulation of a remote start is similar to the demodulation process for the ready portion of an FSM message, except that the space frequency signal that follows a remote start signal distinguishes it from the ready portion of a sync word. When a remote start signal is detected, the +3-volt detector signal goes to 0 volt which causes the integrator (Q16-Q18) output to increase from 0 volt toward +12 volts at an exponential rate. While the integrator output is increasing, the $\overline{\text{MFC}}$ signal goes to −10 volts which causes integrator reset Q15 to generate a positive pulse (−7 volts to 0 volt) that resets the integrator output to +12 volts. When the +3-volt detector goes to −7.5 volts at the end of the remote start signal, the integrator output decreases from +12 volts toward 0 volt at an exponential rate. While the integrator output is decreasing, the MFC signal goes to −10 volts which triggers MFC one-shot multivibrator Q1, Q2 and thereby causes the inverter Q3 output to go to 0 volt. When the integrator output reaches 0 volt and the Q3 output is 0 volt, the output of negative and gate Q13 (remote start) goes to −12 volts. The remote start signal is routed to the self-test function where it is detected to generate a remote stop signal. The remote stop signal is routed back to the receiver and applied to the or gate associated with MFC clamp Q6, Q7, Q8. When the remote stop signal is true (0 volt), the output of the MFC clamp is 0 volt which clamps the output of the MFC one-shot multivibrator to 0 volt. This condition, in turn, causes the output of Q13 (remote start) to go to 0 volt.

Section III. SYNCHRONIZER CIRCUITS, DETAILED FUNCTIONAL ANALYSIS

28. General

(fig. 39)

The synchronizer circuits consist of a receiver relay card, synchronizers No. 1 and No. 2, an IRP and DCP generator, and a 6-kc positive and negative clock pulse generator for receivers A and B. The synchronizer circuits process signals from the PCM and FSM demodulator circuits, to synchronize data to the 6-kc clock pulse and to generate IRP and DCP pulses.

29. Clock Pulse Generation, 6 Kc Positive and Negative

(fig. 39)

The 6-kc clock pulse (CP) generator receives the 6-kc square wave signal from the transmitter subfunction and generates 6-kc positive CP and 6-kc negative CP signals. The generator consists of blocking oscillator Q6, amplifier Q7, and emitter follower Q8 on assembly 1518493, J13A. The positive-going CP are used in synchronizer No. 1, 1518302, J21B and J21C and synchronizer No. 2, 1518303, J20A and J21A. The negative-going CP are used in IRP and DCP generators 593982, J18A and J19A.

a. CP Generation, 6 Kc Negative. The 6-kc square wave signal from the transmitter subfunction is applied to blocking oscillator Q6. The output of the blocking oscillator is a train of 6-kc negative pulses riding at a 0 volt reference and going to −6 volts. The negative CP are routed to the IRP and DCP generators and to inverter Q7.

b. GP Generation, 6 Kc Positive. Transistor Q7 inverts the 6-kc negative pulses and applies them to emitter follower Q8. Emitter follower Q8 current-amplifies the output of Q7 and clamps the lower level of the signal to −12 volts; therefore, the Q8 output is a train of 6-kc, 12-volt, positive pulses riding at a −12-volt reference. The positive CP are routed to the synchronizers.

30. Receiver Relay Card

(fig. 39)

Receiver relay card 1522307 (J20B, receiver A and J19C, receiver B) routes either FSM or PCM signals to the synchronizer circuits. Receiver FSM–PCM select switch S1 controls relays on the card that selects either FSM or PCM signals for processing by the synchronizer circuits. When S1 is in the PCM position, −26.5 volts is applied to the relay coils, energizing them. When S1 is in the FSM position, the −26.5 volts is removed and the relay coils are deenergized. The contacts of relays K3 and K4 are used to select the FSM or PCM signals.

a. Relay K3. Two sets of contacts on K3 are used. Contacts 5 and 2 route $\overline{\text{data}}$ to synchronizer No. 1 when S1 is in the PCM position. When S1 is in the FSM position, contacts 2 and 4 are closed and an open (no signal) is routed to synchronizer No. 1. Contacts 6 and 1 route $\overline{\text{ready}}$ to synchronizer No. 1 when S1 is in the PCM position, and contacts 8 and 6 route $\overline{\text{ready start}}$ to synchronizer No. 1 when S1 is in the FSM position.

b. Relay K4. Two sets of relay K4 contacts are also used. Contacts 2, 4, and 5 route either FSM or PCM $\overline{\text{data}}$ to synchronizer No. 1, and contacts 8, 6, and 1 route either FSM or PCM data to the synchronizer.

31. Synchronizer

(fig. 39)

a. General. The synchronizer consists of ready/ready start detect circuit (F/FSQ5), MOD 8 counter reset circuit (F/FSQ4), MOD 8, 6-kc CP counter circuit (F/FSQ1 through F/FSQ3 and inverter switch Q7), sync data circuits (F/FSQ6), sync data control circuit ($\overline{\text{SP2}}$), IRP command generator circuit, and DCP command generator circuit. All flip-flops in the synchronizer are clocked by 6-kc positive CP (para. 29). The gating at the input to the flip-flops is unique in that the gate inputs must be negative in order for the CP to trigger the flip-flops.

b. Synchronizer Operation. Flip-flops SQ4 and SQ5 decode the sync word portion of the message and their outputs cause the IRP command signal to be generated. An IPR command indicates that message information is about to arrive. When the sync word is decoded, F/FSQ4 resets the MOD 8 counter to a 000 state. The MOD 8 counter then proceeds to count 6-kc positive CP. The MOD 8 counter completes 1 cycle (counts 8 CP) each time slot. At each MOD 8 counter count of 6, a DCP command is generated which marks the center of a data time slot. The be-

ginning of each time slot is marked by the $\overline{SP2}$ signal. Signal $\overline{SP2}$ controls the sync data circuit that synchronizes the data. Figure 10 shows the timing of the synchronizer circuits for FSM messages and figure 11 shows the timing for PCM messages.

32. Synchronizer Logic

(fig. 39)

Synchronizer logic is contained on two assemblies: synchronizer No. 1 1518302 is located in J21B for receiver A and J21C for receiver B; synchronizer No. 2 1518303 is located at J20A for receiver A and J21A for receiver B.

a. Ready/Ready Start Detect F/FSQ5. The logic for F/FSQ5 is as follows:

$$SQ5 = (\text{data receiver } \overline{SQ5}\ \overline{SQ4})\ (CP)$$
$$\overline{SQ5} = (\overline{\text{data}}/\text{open receiver } \overline{\text{ready}}/\overline{\text{ready start receiver}})\ (CP)$$

(1) *PCM operation* (fig. 11). When PCM messages are being received, the $\overline{\text{ready}}/\overline{\text{ready start}}$ receiver signal is $\overline{\text{ready}}$ from the PCM demodulator circuits. The $\overline{\text{data}}$/open receiver signal is $\overline{\text{data}}$ from the PCM demodulator circuits. Both $\overline{\text{data}}$ and $\overline{\text{ready}}$ are at −12 volts at the beginning of time slot 0 which causes the SQ5 signal to go to 0 volt ($\overline{SQ5}$ output to go to −12 volts) at the first CP of time slot 0. Flip-flop SQ5 is not reset until time slot 6, because data and $\overline{SQ4}$ are both 0 volt until this time. Flip-flop SQ5 is reset during time slot 6 (causing the SQ5 output to go to −12 volts) when the data and $\overline{SQ4}$ signals go to −12 volts. Flip-flop SQ5 remains in this state until the $\overline{\text{ready}}$ signal goes to −12 volts in time slot 0 of the following message.

(2) *FSM operation* (fig. 10). When FSM messages are being received, the $\overline{\text{ready}}/\overline{\text{ready start}}$ receiver signal is $\overline{\text{ready start}}$ from the FSM demodulator circuits. The $\overline{\text{data}}$/open receiver signal is open (no signal). The $\overline{\text{ready start}}$ signal goes to −12 volts during time slot 5 which causes the SQ5 signal to go to 0 volt ($\overline{SQ5}$ goes to −12 volts). The SQ5 signal is routed to the FSM demodulator circuit where it causes the $\overline{\text{ready start}}$ signal to go to 0 volt. Flip-flop SQ5 is reset during time slot 6, when data and $\overline{SQ4}$ go to −12 volts, and remains in this state until time slot 5 of the following message.

b. MOD 8 Counter Reset F/FSQ4. The logic for F/FSQ4 is as follows:

$$SQ4 = [(\overline{\text{data}}\ \text{receiver}\ \overline{SQ4})\ (CP)]$$
$$\overline{SQ4} = [(\text{data receiver}\ \overline{SQ5})\ (CP)]$$

During time slot 6, data is −12 volts and SQ5 is 0 volt ($\overline{SQ5}$ is −12 volts); therefore, SQ4 goes to 0 volt with the first CP in time slot 6 because of the $\overline{SQ4}$ logic. When SQ4 goes to 0 volt, signal SQ5 goes to −12 volts on the next CP because of the SQ5 logic. Signal $\overline{SQ4}$ inhibits the MOD 8 counter (*c* below) by resetting the counter flip-flops to zero and holding them in that state until time slot 7 and thus starts the count in synchronization with the new message. Signal SQ4 goes to −12 volts during time slot 7 when $\overline{\text{data}}$ goes to −12 volts. Signal SQ4 is routed to the FSM demodulator circuits where it is used to prevent false ready start signals from being generated.

c. MOD 8 Counter F/FSQ1 Through F/FSQ3. The MOD 8 counter counts 6-kc CP and is reset by counter reset signal $\overline{SQ4}$. The counter counts 8 CP each time slot.

(1) *Counter reset.* Signal $\overline{SQ4}$ is applied to inverter switch Q7 on 1518303, J20A for receiver A (J21A for receiver B). During time slot 6, the $\overline{SQ4}$ signal is negative going and is inverted and applied to F/FSQ1 through F/FSQ3, resetting them to zero (signals SQ1 through SQ3 go to −12 volts). Signal SQ4 is used in the $\overline{SQ1}$ logic; therefore, the counter is inhibited until SQ4 goes to −12 volts during time slot 7.

(2) *MOD 8 counter logic.* The logic for MOD 8 counter F/FSQ1 through F/FSQ3 is as follows:

$$\left.\begin{aligned} SQ1 &= [(\overline{SQ1} + \overline{SQ4})\ (CP)] \\ \overline{SQ1} &= [(SQ1\ \ SQ4)\ (CP)] \end{aligned}\right\} \text{LSD}$$

$$\left.\begin{aligned} SQ2 &= \overline{SQ1}\ \overline{SQ2} \\ \overline{SQ2} &= \overline{SQ1}\ SQ2 \end{aligned}\right\} \text{2d LSD}$$

$$\left.\begin{aligned} SQ3&=\overline{SQ}2\ \overline{SQ}3 \\ \overline{SQ}3&=\overline{SQ}2\ SQ3 \end{aligned}\right\}\ \text{MSD}$$

At the beginning of time slot 7, signal SQ4 goes from 0 volt to −12 volts, which causes the counter to begin its counting action. When signal SQ4 goes to −12 volts, the CP is passed through the CP gate and causes signal $\overline{SQ}1$ to go to −12 volts; thus the counter is synchronized to the 6-kc CP. Each positive-going $\overline{SQ}1$ signal causes F/FSQ2 to change state, and each positive-going $\overline{SQ}2$ signal causes F/FSQ3 to change state. The counter counts from zero to seven each time slot until the next message time slot 6, when it is reset and inhibited ((1) above).

d. Sync Data Control. Sync data F/FSQ6 is controlled by signal $\overline{SP}2$. The logic for $\overline{SP}2$ is as follows:

$$\overline{SP}2=SQ1\ \overline{SQ}2\ SQ3\ SQ4$$

Signal SQ4 is at −12 volts for each time slot of the message frame except for a 1.33 msec interval during the sync word. Signals SQ1, $\overline{SQ}2$, and SQ3 are all at −12 volts once every 750-cps period (time slot). The −12-volt $\overline{SP}2$ signal is current-amplified by emitter follower Q8 and routed to F/FSQ6 on 1518302, J21B for receiver A (J21C for receiver B).

e. Sync Data F/FSQ6. The logic for F/FSQ6 is as follows:

$$SQ6=[(\overline{SP}2\ \text{data rcvr})\ (CP)]$$

$$\overline{SQ}6=[(\overline{SP}2\ \overline{\text{data}}\ \text{rcvr})\ (CP)]$$

Signal SQ6 follows the data receiver signal. Signal $\overline{SQ}6$ is the logical complement of the data receiver signal, and it is routed through inverter and logic level changer Q9, CR31 to the associated input buffer as sync data. The inverter and logic level changer invert and clamp the sync data signal to 0 volt and −6 volts. A 0-volt signal indicates a true data bit and a −6-volt signal indicates a false data bit.

f. IRP Command. The logic for the IRP command on assembly 1518303, J20A for receiver A (J21A for receiver B) is as follows:

$$\text{IRP command}=\overline{SQ}4\ \overline{SQ}5$$

Signals $\overline{SQ}4$ and $\overline{SQ}5$ are both −12 volts for one 6-kc CP period during time slot 6. The Q9 output is at −6 volts until the $\overline{SQ}4$ and $\overline{SQ}5$ signals go to −12 volts and then the Q9 output goes to 0 volt. This signal is routed to the IRP and DCP generator 593982, J18A for receiver A (J19A for receiver B), where the input ready pulse is generated (para. 33).

g. DCP Command. The logic for the DCP command on assembly 1518303, J20A for receiver A (J21A for receiver B) is as follows:

$$\text{DCP command}=\overline{SQ}2\ \overline{SQ}3\ SQ4\ SQ1$$

This logic equation is true ($\overline{SQ}2$, $\overline{SQ}3$, SQ4, and SQ1 at −12 volts) once each time slot, except for time slot 6, for one 6-kc CP time, 750 times per second. The output of the transistor and gate and logic level changer Q10, Q11 is −6 volts until the equation is true and then it goes to 0 volt for one CP period. The output is routed to the IRP and DCP generator where the DCP is generated (para. 33).

33. IRP and DCP Generator

(fig. 39)

a. IRP Generator. The IRP generator is located on assembly 593982, J18A for receiver A (J19A for receiver B), and consists of pulse gate CR1–CR2 and blocking oscillator Q1. The IRP generator receives the IRP command from synchronizer No. 2 (para. 32*f*) and 6-kc negative CP from 1518493, J13A. The pulse gate applies one CP to the blocking oscillator when the IRP command is true (0 volt). The blocking oscillator output is a negative pulse (0 to −6 volts) which is routed to the associated input buffer to signal the beginning of a new message.

b. DCP Generator. The DCP generator consists of pulse gate CR7, CR8, and blocking oscillator Q2 on 593982, J18A for receiver A (J19A for receiver B). The DCP generator receives the DCP command from synchronizer No. 2 (para. 32*g*) and the 6-kc CP from 1518493, J13A. The pulse gate applies one CP to the blocking oscillator each time the DCP command is true. The output of the blocking oscillator is a series of 0- to −6-volt pulses at 750 pps. The DCP is routed to the associated input buffer to mark the center of a time slot.

CHAPTER 4

TRANSMITTER SUBFUNCTION, DETAILED FUNCTIONAL ANALYSIS

Section I. FSM MESSAGE MODULATION

34. General

(fig. 40)

Ready control and data control signals are received from an output buffer in the form of serial binary pulses. The rate is controlled by the 750-pps T-pulses generated in the transmitter subfunction and routed to the associated output buffer to synchronize the ready control and data control signal. A complete FSM message is 83 time slots (1.33-millisecond intervals) long and contains all the information on a given track. The ready control signal is part of the sync word, and it is true for four time slots at the beginning of the message. The data control signal is a series of digital pulses, one for each true bit (one time slot) in the message. The data and ready control signals are anded with square waves that have a repetition rate that is 32 times the frequency of the output mark, space, or midfrequency signals. The gated frequency is divided by 32, filtered, and routed to the output buffers as the FSM modulated message.

35. Modulator Gate and Oscillators

(fig. 40)

Modulator gate and oscillator 1518471, J7A, consists of three free-running oscillators (36 kc, 60 kc, and 48 kc), mark, space, and midfrequency and gates, or gate, and an emitter follower.

a. Oscillators, 36 Kc, 60 Kc, and 48 Kc. The 36-kc, 60-kc, and 48-kc oscillators are free-running, crystal-controlled oscillators that generate square wave output signals at the specified frequency. The 36-kc oscillator output is 32 times the mark frequency and is routed to mark gate Q3. The 60-kc oscillator output is 32 times the space frequency and is routed to space gate Q7 and emitter follower Q6. The 48-kc oscillator output is 32 times the midfrequency and is routed to midfrequency gate Q8 and to emitter follower Q11.

b. Mark Gate. Data, $\overline{\text{ready}}$, and 36-kc square wave signals are anded in mark gate Q3. The data signal comes from the associated output buffer. A ready control signal from the associated output buffer is routed through inverter Q10 on 1518493, J13A to generate the $\overline{\text{ready}}$ signal. When there is a true data bit in the FSM message from the associated output buffer, the 36-kc square wave signal is passed through mark gate Q3 to composite gate Q9.

c. Space Gate. Data, $\overline{\text{ready}}$, and 60-kc square wave signals are anded in space gate Q7. $\overline{\text{Ready}}$ is generated as explained in *b* above. A data control signal from the associated output buffer is routed through inverter Q9 on 1518493, J13A to generate the $\overline{\text{data}}$ signal. When there is a space (data and ready false) in the FSM message from the associated output buffer, the 60-kc square wave signal is passed through space gate Q7 to composite gate Q9.

d. Midfrequency Gate. Midfrequency gate Q8 ands the ready control signal from the associated output buffer with the 48-kc square wave signals from the 48-kc oscillator. When the ready control signal is true, the 48-kc square wave signals are passed through the and gate to composite gate Q9.

e. Composite Gate. The outputs of the space, mark, and midfrequency gates, only one of which can be true at any specific time, are applied to composite gate Q9. When one of the inputs to Q9 is true, the output of the composite gate is a series of 36-kc square wave signals representing the mark frequency, 60-kc square wave signals representing the space frequency, or 48-kc square wave signals representing the midfrequency. The output of composite gate Q9 is routed to frequency divider 1518494, J8A.

f. Emitter Follower Q11. Emitter follower Q11 current-amplifies the 48-kc square wave signals

from the 48-kc oscillator, and routes them to frequency divider, 1518494, J9A. The frequency of the square wave signals is divided to generate a 6-kc square wave output signal and a 1,500-cps square wave output signal (para. 40).

36. FSM Frequency Division

(fig. 40)

The 60/48/36 kc square wave signals from composite gate Q9 on 1518471, J7A are applied to divide-by-two multivibrator Q1, Q2 on 1518494, J8A that supplies 30/24/18 kc square wave signals to divide-by-two multivibrator Q3, Q4. Multivibrator Q3, Q4, supplies 15/12/9 kc square wave signals to divide-by-two multivibrator Q5, Q6. The 7.5/6/4.5 kc square wave signals from Q5, Q6 are divided by two by multivibrator Q7, Q8 and supply 3,750/3,000/2,250 cps square wave signals to divide-by-two multivibrator Q9, Q10. The Q9, Q10 output is a series of square wave signals: 1,875 cps for space frequency, 1,500 cps for midfrequency, and 1,125 for mark frequency. The Q9, Q10 output is applied to differential amplifier Q11, Q12. Amplifier Q11, Q12 provides dc amplification and isolation between the frequency divider and the modulator output filter (para. 37), and presents a constant impedance to the filter. The Q11, Q12 square wave output of frequency divider 1518494, J8A is routed to modulator relay K2 on 1522312, J12A as the FSM modulator signal.

37. Modulator Output Filter

(fig. 40)

The modulator output filter is located on assembly 1518484, J10A–J11A. The filter changes the 1,875/1,500/1,125 cps square wave signals (FSM modulator signal) to sine wave signals. The FSM modulator signal from the frequency divider is routed through contacts 4–2 of deenergized relay K2. Relay K2 is deenergized when the transmitter is operating in FSM (para. 41). The K2 output (FSM/PCM modulation input) is applied to filter FL1 on 1518484, J10A–J11A. Filter FL1 filters its square wave input signal and produces a sine wave output signal, which is the FSM transmitted message. The sine wave output (filter output) is routed through another set of modulator relay K2 contacts to attenuation switches on 1518484, J10A–J11A as the attenuated input signal.

38. FSM Message Attenuation and 750-PPS T-Pulse Generation

(fig. 40)

a. The attenuated input signal is applied to switch S1 on 1518484, J10A–J11A. The message is applied from S1 either direct to switch S2 or through 2-db attenuator R1–R3 to S2. The message is then applied from S2 either direct to switch S3 or through 2-db attenuator R4–R6 to S3, and then to output transformer T1 through an 8-db isolation pad (R10–R12), or through a third 2-db attenuator (R7–R9); therefore, attenuation switches S1–S3 provide 0 to 6-db attenuation in 2-db steps. The 8-db isolation pad provides a constant impedance at the modulator output. Output transformer T1 couples the modulated message to the output lines through transmitted message relay K1. Relay K1 is located on assembly 1522312, J12A and is deenergized when the transmitter is operating in FSM mode (para. 41).

b. The 750-pps T-pulse generator supplies 750-pps timing pulses to the output buffer to synchronize the transmitted message. The generator consists of emitter follower Q1, shaper Q2, divide-by-two multivibrator Q3, Q4, and blocking oscillator Q5. The 750-pps T-pulses are generated in both FSM and PCM modes. In FSM operation 1,500-cps square wave signals from frequency divider 1518494, J9A are routed through level changer R13, R14 and closed contacts 8–6 of relay K3 on 1522312, J12A to emitter follower Q1 on 1518493, J13A. Level changer R13, R14 provides the triggering level for the T-pulse generator in the FSM mode. Emitter follower Q1 isolates and current-amplifies the 1,500-cps square wave signals and routes them through shaper Q2 to divide-by-two multivibrator Q3, Q4. Transistor Q2 amplifies and clips the square wave signal to sharpen the leading and trailing edges for proper triggering of the multivibrator. The output of the multivibrator is a 750-cps square wave signal that triggers blocking oscillator Q5. The signal output of Q5 is the 750-pps T-pulses. In the FSM mode, these pulses are referenced to −12 volts by the mode control signal routed from pin 2 of relay K3 on 1522312. In the PCM mode, these pulses are referenced to 0 volt; thus a PCM or FSM signal is provided, in addition to the 750-pps T-pulses, on the same line to the output buffer.

Section II. PCM MODULATION

39. General

(fig. 40)

For PCM modulation, data control signals from an output buffer are modulated with a 1,500-cps sine wave signal. The data control signal is in serial binary form and contains all the information on a track. The data control signal has a bit rate of 750 bps. This rate is a result of the 750-pps T-pulses (para. 44) that are routed to the associated output buffer. A ready control signal (also routed from the output buffer) is present for the first 3 bit intervals of the message. The ready control signal is modulated, in the PCM transmitter circuits, with 600-cps sine wave signals and mixed with the first 3 data bits to form the ready word. A complete PCM message is 82 bits long. The circuits used in modulating the PCM message include a frequency divider that divides a 48-kc square wave signal by 32 to develop 1,500-cps square wave signals, a variable gain amplifier that gates 2 cycles of 1,500 cps for each true data control signal, and a 600-cps oscillator and modulator that gates and mixes the 1,500- and 600-cps sine wave signals. Relays route the modulated PCM message to the output communication lines.

40. Sine Wave Generation, 1,500 Cps

(fig. 40)

The 48-kc square wave signal output from emitter follower Q11 on 1518471, J7A (para. 35) is 32 times the frequency of 1,500 cps. The 48-kc signal is applied to a frequency divider that is composed of five divide-by-two multivibrators. The 48-kc signal is divided down to 6 kc in the three divide-by-two multivibrators Q1, Q2; Q3, Q4; and Q5, Q6. Two outputs are taken from divide-by-two multivibrator Q5, Q6. Both outputs are 6-kc square wave signals. One output is routed to the synchronizer circuits in the receiver subfunction where it is used to generate clock pulses; the other output is applied to divide-by-two multivibrator Q7, Q8. The Q7, Q8 output is a 3-kc square wave signal that is applied to the final divide-by-two multivibrator (Q9, Q10). The Q9, Q10 output is a 1,500-cps square wave signal that is applied to differential amplifier Q11, Q12. Amplifier Q11, Q12 provides dc amplification and isolation between the frequency divider and the following circuits and presents a constant impedance to filter FL1 on 1518484, J10A–J11A. The 1,500-cps square wave signal is applied to filter FL1 on modulator output 1518484, J10A–J11A through modulator relay K2 on 1522312, J12A. Relay K2 is energized when operating in PCM (para. 41). Filter FL1 changes the 1,500-cps square wave signal into a 1,500-cps sine wave signal. The 1,500-cps sine wave signal is applied to variable gain amplifier and transmitter relay card 1522312, J12A.

41. Relays K1, K2, K3, and K4

(fig. 40)

The transmitter subfunction contains four relays that control the signal flow through the subfunction in PCM or FSM mode. The relays are located on assembly 1522312, J12A and are energized by TRANSMITTER FSM/PCM selector switch S1. Switch S1 is a two-position switch. With S1 in the FSM position, the four relays are deenergized and their contacts are in the position shown on figure 41. With S1 in the PCM position, −26.5 volts from the power supply subfunction is applied to the four relays and causes them to become energized.

a. Relay K1. Relay K1 is the transmitted message relay, and it controls the routing of the modulated FSM or PCM message to the output lines. FSM messages are routed from modulator output 1518484, J10A–J11A (para. 38). PCM messages are routed from 600-cps oscillator and modulator 549591, J14A–J17A (para. 43).

b. Relay K2. Relay K2 is the modulator relay that controls the input to modulator output filter FL1 on 1518484, J10A–J11A (paras. 37 and 40) and the input to T-pulse relay K3 and the PCM modulator circuit on 1522312, J12A (para. 42).

c. Relay K3. Relay K3 is the T-pulse relay. The T-pulse relay controls the reference voltage level of the 750-pps T-pulses and also the routing of 1,500-cps square wave signals or 1,500-cps, sine wave signals to the T-pulse generator located on 1518493, J13A (para. 44).

d. Relay K4. Relay K4 is the FSM/PCM control relay. It provides logic level signals to indicate the transmitter operating mode; however, these signals are not used.

42. PCM Data Modulation

(fig. 40)

The 1,500-cps sine wave signal from filter FL1 (para. 40) is applied to switch Q1 on 1522312, J12A through closed contacts 6–1 of relay K2. The information to be modulated (data control from the associated output buffer) is also applied to switch Q1. Each time the data control signal goes true, 2 cycles of the 1,500-cps signal is passed to emitter follower Q2 through LEVEL CONTROL R5. When the data control signal is false, the 1,500-cps signal is inhibited by switch Q1. LEVEL CONTROL R5 adjusts the signal level into emitter follower Q2 and thereby adjusts the gain of amplifier Q3. Emitter follower Q2 current-amplifies the 1,500-cps signal and routes it to amplifier Q3. The 1,500-cps signal (modulated data) is amplified by Q3 and routed to 600-cps oscillator and modulator 549591, J17A–J17A as 1,500-cps modulated data.

43. Oscillator and Modulator, 600 Cps

(fig. 40)

a. General. The 600-cps oscillator and modulator consists of an oscillator section, amplifier section, gating section, modulator section, and a 600-ohm line driver section. The 600-cps oscillator and modulator generates 600-cps sine waves, mixes (modulates) 600-cps and 1,500-cps signals, and gates out three time slots of 600 cps and 1,500 cps for the ready control signal from the associated output buffer, and 2 cycles of 1,500-cps signals for each true data bit. A 600-ohm line driver presents a constant 600-ohm impedance to the output lines.

b. Oscillator Section. The oscillator section consists of a 600-cps oscillator Q1, Q3, Z1, 600-CPS AMPL ADJ R6, and amplifier Q2. The 600-cps oscillator is a free-running oscillator that has a resonant frequency of 600 cps. The output of the oscillator is a 600-cps sine wave that is applied to amplifier Q2 through 600 CPS AMPL ADJ R6. Resistor R6 adjusts the signal level into amplifier Q2, thereby adjusting the gain of the amplifier. The amplified output of Q2 is applied to modulator Q4, T1, T2.

c. Gating Section. The gating section consists of 200-cps low filter FL1 and gate Q5. The ready control signal from the associated output buffer is true for three time slots at the beginning of each transmitted word. The ready control signal is applied to gate Q5 through filter FL1. Filter FL1 prevents the generation of unwanted line transients in the modulator by rounding the edges of the ready control signal. Gate Q5 controls the mixing of the 600-cps signal and the 1,500-cps signal in the modulator. When the ready control signal is true, Q5 permits the 600- and 1,500-cps signals to be mixed.

d. Modulator Section. The modulator section consists of Q4, T1 and T2. When the ready control signal is true, gate Q5 permits 600-cps signals to be applied to the 600-ohm line driver section and mixed with 1,500-cps signals. When the ready control signal is false, Q5 inhibits the 600-cps signal and only 1,500 cps is applied to the 600-ohm line driver section.

e. Line-Driver Section, 600 Ohms. The 600-ohm line-driver section consists of Q6, Q7, and T3. It mixes (at the beginning of a message) and amplifies the message and provides a constant 600-ohm line impedance. Two cycles of the 1,500-cps signal are applied to the line driver each time there is a true data bit in the data control signal. A 600-cps signal is also applied to the line driver for 3 time bits when the ready control signal is true at the beginning of a message. At this time, both the 1,500-cps and 600-cps signals are present at the input to the line driver where they are mixed and sent out. The output of the line driver is routed through closed contacts 5–2 and 1–6 of transmitter message relay K1 (para. 41) to the lines as the modulated message.

44. PCM 750-Pps T-Pulse Generation

(fig. 40)

The 750-pps T-pulse generator supplies 750-pps timing pulses to the output buffer to synchronize the transmitted message. The generator consists of emitter follower Q1, shaper Q2, divide-by-two multivibrator Q3, Q4, and blocking oscillator Q5. The 750-pps T-pulses are generated in both FSM and PCM modes. The operation of the 750-pps T-pulse generator in the PCM mode is identical with that of the FSM mode as explained in paragraph 38*b*, except that the 1,500-cps T-pulse command signal is routed through filter FL1 on 1518484, and the filter generates sine wave signals instead of square wave signals. The filter output is routed through closed contacts of relay K3 on 1522312 to the 750-pps T-pulse generator. The mode control signal is also routed from relay K3 and is ground (0 volt) in the PCM mode. Therefore, the 750-pps T-pulses from the T-pulse generator are referenced to ground when operating in the PCM mode.

CHAPTER 5

POWER SUPPLY SUBFUNCTION, BLOCK DIAGRAM ANALYSIS

45. General
(fig. 41)

The power supply subfunction consists of a filter card, +18-volt regulator, −27-volt regulator, +27-volt regulator, and +12-volt unregulated power supplies, and +12-volt regulators and protection circuits. Filtered and regulated power is routed to all assemblies as shown on the transmitter-receiver unit schematic diagram (fig. 12).

46. Filter Card
(fig. 41)

Filter card 547885, J1B, filters dc voltages from system power supplies (TM 11-5840-273-30). These dc voltages are +1.5 volts, −6 volts, −7.5 volts, −28 volts, +28 volts, +150 volts, +300 volts, +50 volts, and −50 volts. The filter shunts to ground any noise that may have been generated on the lines.

47. Plus 18-Volt Regulator
(fig. 41)

Diode CR4 contained on assembly 1518484, J10A–J11A, is the +18-volt regulator. Plus 50 volts from the filter card is applied to CR4. The output of CR4 is a constant +18 volts. The routing of the regulated −27 volts is shown in figure 12.

48. Minus 27-Volt Regulator
(fig. 41)

Diode CR3 contained on assembly 1518484, J10A–J11A, is the −27-volt regulator. Minus 50 volts from the filter card is applied to CR3. The output of CR3 is a constant −27 volts. The routing of the regulated −27 volts is shown in figure 12.

49. Plus 27-Volt Regulator
(fig. 41)

Diode CR5 on assembly 549591, J14A–J17A is the +27-volt regulator. Plus 50 volts from the filter card is applied to CR5. The output of CR5 is a constant +27 volts. The routing of the regulated +18 volts is shown in figure 12.

50. Plus and Minus 12-Volt Unregulated Power Supplies
(fig. 41)

The ±12-volt unregulated power supplies are located on assembly 1512530, J1A–J5A. The power supplies generate ±24 volts and route this voltage to the ±12-volt regulators.

a. Minus 12-Volt Unregulated Power Supply. The −12-volt unregulated power supply consists of the primary and one of the secondaries of transformer T1, bridge rectifier CR17–CR20, fuse F2, and filter C14. The 120 volts ac 400 cps is applied to stepdown transformer T1 from system power. The 120 volts ac is stepped down to approximately 54 volts peak-to-peak. The 54 volts is applied to bridge rectifier CR17–CR20. The bridge is a full-wave rectifier so that the output is a pulsating signal approximately 24 volts. The pulsating 24-volt signal is filtered by C14 where the ripple is removed, resulting in a −24-volt level. The −24 volts is routed to the −12-volt regulator (para. 51) and also to assemblies in the transmitter-receiver as shown on figure 12. Fuse F2 is provided to protect the unregulated power supply from overloads.

b. Plus 12-Volt Unregulated Power Supply. The +12-volt unregulated power supply consists of the primary and one of the secondaries of transformer T1, bridge rectifier CR13–CR16, fuse F1, and filter C13. The operation of the +12-volt unregulated power supply is identical with that of the −12-volt supply except that different polarities are used.

51. Voltage Regulators, ±12 Volts
(fig. 41)

The operation of both the ±12-volt regulators is identical; therefore, only the +12-volt regulator

is explained. The +12-volt regulator consists of a voltage control multivibrator circuit, series switch circuit, and an output filter and overvoltage protector circuit. An overload protector circuit is also included to protect the regulator in case of excessive current flow.

a. Regulation. The unregulated dc voltage from the unregulated supply (approximately 24 volts) is applied to +12-volt switch Q13. The ratio of on-time to off-time of the switch determines the average current supplied to the output filter. The on-time and off-time of switch Q13 is controlled by the voltage control multivibrator circuit through switch driver Q11 and switch turnoff Q10.

(1) *Voltage control multivibrator circuit.* The voltage control multivibrator circuit consists of reference voltage power supply C3, CR3, voltage adjust R12, differential amplifier Q4, Q8, constant current source Q6, multivibrator Q5, Q7, and multivibrator turn-on Q9, CR8, CR9. Differential amplifier Q4, Q8 compares the voltage from the output filter with the adjusted reference voltage generated by the reference voltage power supply. Voltage adjust R12 is set so that the reference voltage causes a constant +12 volts at the output of the regulator. The differential amplifier controls the switching of multivibrator Q5, Q7. The multivibrator has a nominal frequency of about 45 kc but on and off periods are not equal. The ratio of the positive and negative portions of the square wave output determines the output voltage of the output filter. Constant current source Q6 provides a constant current to differential amplifier Q4, Q8. Multivibrator turn-on Q9, CR8, CR9 eliminates the problem that arises when both transistors in the multivibrator go into saturation when power is initially applied. If both transistors saturate at initial turn-on, Q9, CR8, CR9 remove the supply voltage from constant current source Q6 which turns off both transistors in the multivibrator. The multivibrator then starts its normal switching action and Q9 reapplies the supply voltage to the constant current source. The square wave output of multivibrator Q5, Q7 is applied to switch driver Q11 and switch turnoff Q10 in the series switch circuit.

(2) *Series switch circuit.* The series switch circuit consists of switch driver Q11, switch turnoff Q10, and +12-volt switch Q13. The positive-going portion of the square wave from the multivibrator turns on switch driver Q11 which then turns on +12-volt switch Q13. Switch turnoff Q10 removes the stored base charge of +12-volt switch Q13 and speeds up the turnoff of Q13 when the multivibrator output pulse is negative going; therefore, Q13 is turned on and off by the multivibrator output. The Q13 output is a chopped dc signal and is applied to the output filter and overvoltage protection circuit.

(3) *Output filter and overvoltage protection circuit.* The Q13 output is applied across output filter L1, C9, C10, R30. The filter smooths the voltage and supplies the +12-volt regulated output. Protector CR21 is an overvoltage protector that limits the output voltage to +15 volts.

b. Overload Protection Circuit. The overload protection circuit consists of Q1, Q2, Q3, S1, and R9. The overload protection circuit senses the voltage across R9 through which all the current from the unregulated supply flows. If the output current exceeds 800 milliamperes, the overload protection circuit holds the base and emitter of switch driver Q11 at the same ground potential. When Q11 is not conducting, +12-volt switch Q13 does not supply current to the output filter, and no current is delivered to the load. Switch S1 resets supply by breaking the lockup circuit. If the overload still exists, the cycle is repeated.

CHAPTER 6

DETAILED CIRCUIT ANALYSIS

Section I. TRANSMITTER SUBFUNCTION

52. Oscillator and Modulator, 600 Cps, 549591

(fig. 14)

a. General. The 600-cps oscillator and modulator (549591) consists of an oscillator section, an amplifier section, a modulator section, a line driver section, and a low-noise power circuit. The oscillator is a free-running, 600-cps, tuned oscillator. The oscillator output is applied to a voltage divider which includes 600-CPS AMPL ADJ R6. The 600 cps from R6 is amplified and supplied to the modulator. The modulator gates the 600-cps signal with the 600-cps modulator control signal to generate a pulse code modulated signal that is three time slots in duration. The 600-cps signal from the modulator is mixed with the 1,500-cps signal, from the 1,500-cps modulator circuit on 1522312, at the input to the 600-ohm line driver which amplifies the mixed signal and supplies it to the line. Low-noise power for some bias voltages is generated internally and for other bias voltages is supplied by modulator output 1518484.

b. Oscillator Circuit, 600 Cps. When power is applied, both Q1 and Q3 are forward-biased and begin to conduct. The initial current through Z1, a parallel-tuned LC circuit, causes the tank circuit to oscillate at its resonant frequency (600 cps), and the resulting signal is coupled back to Q1 by C4 and R9. Transistor Q1 amplifies the signal and drives Q3 which sustains Z1 oscillations.

(1) *Feedback amplifier Q1.* Voltage divider R3, R4 forward-biases Q1 and provides it with a constant bias. Emitter resistor R8 provides degenerative feedback for stability. Additional negative feedback is supplied through R4. Resistor R7 is collector load resistor. The output of Q1 is coupled by capacitor C1 to the base of Q3.

(2) *Tuned amplifier Q3.* The output of Q1 is amplified by Q3 and supplied to the amplifier section. It is also fed back through coupling network C4, R9 to the base of Q1. Filter Z1, which is resonant at 600 cps, makes the gain of Q3 maximum at 600 cps, with the result that the output of Q3 is a 600-cps sinusoidal voltage. Voltage divider R10, R12 provides Q3 with a constant forward bias. Capacitor C2, and diodes CR1 and CR2 provide a shunt impedance across the input to Q3 that varies as a function of temperature. This condition provides temperature compensation for Q3, which insures gain stability. Emitter resistor R19 and resistor R12 provide degenerative feedback, which also contributes to gain stability. Low-pass filter R18, C3 acts as a decoupling network to keep noise from the tuned amplifier affecting the +27-volt regulated bias voltage. Coupling network R9, C4 provides regenerative feedback to promote sinusoidal oscillation. The oscillator output can be observed at TP2.

c. Amplifier Circuit. The oscillator output is applied to a voltage divider consisting of resistor R5 and 600 CPS AMPL ADJ R6. The 600 CPS AMPL ADJ (R6) is normally adjusted for 9 volts peak-to-peak at the output of the modulator. The 600-cps output of R6 is amplified by Q2 and the output of Q2 is applied to emitter follower Q4. The output of Q4 drives the input transformer of the modulator.

(1) *Amplifier Q2.* The 600-cps signal output of R6 is coupled by capacitor C5 to the base of Q2. The amplified 600 cps is supplied through coupling capacitor C6 to the base of Q4. Voltage divider R11,

R13 forward-biases the base of Q2. Degenerative feedback for gain stability is supplied through R13 and by emitter resistor R15. Resistor R14 is the collector load resistor.

(2) *Emitter follower Q4.* The 600-cps signal from Q2 is current-amplified by Q4 which drives T1. Voltage divider R16, R17 provides the proper bias for Q4. Resistor R20 is the emitter load resistor and C7 provides dc isolation for T1.

d. Modulator Circuit. The 600-cps signal from Q4 is always present at modulator input transformer T1. The 600-cps modulator control signal (ready xmtr) is modified by low-pass filter FL1 to drive modulator gate Q5. Gate Q5 controls the output of modulator output transformer T2 by either forward-biasing or back-biasing switching diodes CR3 and CR4.

(1) *Modulator gate Q5.* The modulator control signal is 0 volt for three time slots at the beginning of each message and −15 volts at all other times. The modulator control signal may be observed at TP1 and is applied to 200-cps, low-pass, Pi-type filter FL1. Filter FL1 removes high frequency components from the incoming signal that degrade the risetime and falltime of the pulse supplied to Q5, and minimize transient effects in T2. The output of Q5 is taken across emitter resistor R23 and varies from −0.6 volt to −15.5 volts. Base resistor R22 limits Q5 base current to avoid signal distortion. The output of Q5 is applied to the center tap of the T2 primary.

(2) *Modulator.* The secondary of T1 has its center tap biased to −4.8 volts by voltage divider R24, R25. This forward-biases CR3 and CR4 when the output of Q5 is −0.6 volt and reverse-biases them when Q5 output is −15.5 volts. When CR3 and CR4 are forward-biased, the 600-cps signal (about 9 volts peak-to-peak) controls the current through each diode, and therefore, the current through each half of the T2 primary. When this condition occurs, there is a 600-cps output across the secondary of T2. The secondary of T2 is connected to the −4.2-volt bias. Resistor R32 limits Q6 base current and R31 prevents transformer ringing by approximating the transformer output impedance.

e. Line Driver Circuit, 600 Ohm. The modulated 600-cps and 1,500-cps signals are mixed through a resistor network, amplified by Q6 and routed to Q7, which current-amplifies the mixed signal and drives T3. Mixer amplifier Q6 is biased for class A operation by −4.2 volts from voltage divider, filter C12, R35, and R36.

(1) *Mixer amplifier Q6.* The 600-cps and 1,500-cps modulated signals are mixed by resistor network R31, R32 and applied to the base of Q6. The mixed and amplified signal is supplied through coupling capacitor Q9 to the base of Q7. Low-pass filter capacitor C8 attenuates transients. Emitter resistors R27 and R28 are current-limiting resistors. Resistor R27 provides stabilizing degeneration. Capacitor C10 is an emitter bypass capacitor which eliminates degeneration that would normally be caused by R28. The collector load resistor is R26.

(2) *Driver Q7.* The output of Q6 is current-amplified by Q7 to drive T3. Voltage divider R29, R30 biases the base of Q7 to +6 volts. Resistor R33 is the emitter load resistor and capacitor C11 provides dc isolation for T1. Precision resistor R34 provides a removable (by use of the shorting line) 3-decibel (db) attenuation of the output signal. The signal across the primary of T3 can be observed at TP4. The output impedance of T3 is 600-ohms, which matches the communications lines.

f. Low-Noise Power Circuit. Low-noise +27-volt regulated power is developed across CR5. Resistor R1 is the current-limiting resistor for CR5. Low-noise +22-volt regulated power is developed across CR6. Resistor R2 is the current-limiting resistor for CR6.

53. Modulator Gate and Oscillator, 1518471 (fig. 25)

This assembly contains three nearly identical oscillators, two emitter followers, three similar and gates used to gate the outputs of the oscillators, and a composite gate used to sum the outputs of the and gates. The and gates and their input signals are so arranged that no two oscillator outputs are gated out at the same time.

a. Oscillator, 48 Kc. The initial application of power to this circuit causes crystal Y3 to oscillate slightly. The sinusoidal signal resulting from these oscillations is coupled through base current-limiting resistor R27 to the base of transistor Q12. The base of Q12 is biased to about −0.5 volt by biasing resistor R38. The amplified sinusoidal signal, which appears on the collector of Q12, is coupled to the base of Q10 by feedback capacitor C5. Transistor Q10 is held in an active, conducting state by a negative voltage applied to its base by the voltage divider consisting of collector resistor R30, feedback resistor R34, and bias resistor R35. The sinusoidal signal appearing on the base of Q10 is of sufficient amplitude to drive Q10 alternately into cutoff and saturation. The amplified square wave signal that appears on the collector of Q10 is of sufficient amplitude and correct phase to reinforce the oscillations of crystal Y3. The tuned circuit formed by L3 and C6 suppresses harmonics at the base of Q12 by providing a high impedance at the crystal frequency (48 kc) and a low impedance at all other frequencies.

b. Oscillators, 36 Kc and 60 Kc. The 36-kc oscillator and the 60-kc oscillator are nearly identical with the 48-kc oscillator. The following charts outline the differences and the similarities of the three oscillators:

(1) *Chart of dissimilar components.*

Oscillator	Crystal	Frequency (kc)	Capacitor	Value ($\mu\mu$f)
36 kc	Y1	36	C2	8,200
48 kc	Y3	48	C6	4,300
60 kc	Y2	60	C4	2,700

(2) *Chart of similar components.*

36-kc osc	48-kc osc	60-kc osc
Q1	Q10	Q4
Q2	Q12	Q5
R5	R34	R18
R6	R45	R19
R7	R37	R20
R8	R38	R21
R9	R39	R22
C1	C5	C3
L1	L3	L2

c. Emitter Followers, Q11 and Q6. Emitter follower Q11, with R33 used as an emitter load resistor, current-amplifies the output of the 48-kc oscillator. Diode CR2 clamps the output of Q11 so that it cannot go more negative than −12 volts. Emitter follower Q6, which uses R17 as an emitter resistor and diode CR1 as a clamping diode, operates in the same manner as Q11. It current-amplifies the 60-kc oscillations. Its output, however, is not used.

d. Midfrequency And Gate, Q8. When either the ready transmitting signal or the output of the 48-kc oscillator is a negative voltage, the output of the summing network (which consists of bias resistor R27, logic input resistor R26, and oscillator input resistor R28) is sufficiently negative to forward-bias the base-emitter junction of Q8 and causes it to conduct. Transistor Q8 collector current, flowing through collector resistor R29, causes the collector voltage to drop to about 0 volt. Thus, when ready transmitter signal is at −15 volts the output of the oscillator has no effect on the output of Q8. When the ready transmitter signal is at 0 volt, however, the output of the oscillator, which varies between 0 volt and −12 volts, causes Q8 to alternate between cutoff and saturation; thus the output of Q8 is an inverted replica of the oscillator output when the ready transmitter signal is 0 volt.

e. Mark And Gate Q3 and Space And Gate Q7. And gates Q3 and Q7 operate as described for the midfrequency and gate (*d* above). The following is a chart of similar components:

Midfrequency and gate Q8	Mark and gate Q3	Space and gate Q7
R26	R10	R11
R26	R1	R23
R27	R2	R12
R28	R3	R13
R29	R14	R24
Q8	Q3	Q7

f. Composite Gate Q9. The composite gate consists of a summing network, which includes input resistors R16, R25, and R31, and an amplifier (Q9). The output of any one of the and gates, switching between 0 volt and −12 volts, is coupled through an input resistor and provides a sufficient

change in voltage on the base of Q9 to drive Q9 alternately to cutoff or saturation. When the output of one of the and gates is a square wave signal, the outputs of the other two and gates are 0 volt; thus the output of Q9 is a square wave signal (0 volt to −12 volts), the frequency of which is the same as one of the oscillators.

54. Modulator Output, 1518484

(fig. 26)

The modulator output consists of a bandpass filter, attenuator networks, an isolation transformer, surge suppression diodes, and voltage regulator diodes. Modulated square wave messages from the modulator gate and oscillator (1518471) circuits, after being frequency divided, are fed into low-pass filter FL1 through coupling capacitor C1. Filter FL1 suppresses unwanted harmonics of the incoming square wave signal. The output of FL1 is a sinusoidal signal which, after passing through relay contacts in another circuit, becomes the attenuator input. The attenuator consists of three attenuator pads in series, which may be individually bypassed by S1–S3. The output from the attenuators is applied to a T-pad having an additional loss of 8 db. The attenuators have a possible total loss of 20 db, the first 12 db of which can be switched in or out. Isolation transformer T1 couples the modulated message to a 600-ohm line. Diodes CR1 and CR2 are surge suppression diodes which protect the circuit against high voltage surges which may occur on the output line. Diodes CR3 and CR4 are voltage-regulator diodes. They break down when the voltage between their anode and cathode reaches 12 volts. Resistor R13 and diode CR3 derive the regulated −27-volt output from the −50-volt supply voltage. Current-limiting resistor R13 allows approximately 100 milliamperes (ma) to flow in the regulated −27-volt output. Resistor R14 and diode CR4 derive the regulated +18-volt output from the +50-volt supply voltage. Current-limiting resistor R14 allows approximately 40 ma to flow in the +18-volt regulated output.

55. CP Generator, 6 Kc and 750 Pps, 1518493

(fig. 28)

The 6-kc and 750-pps CP generator consists of a T-pulse generator, a 6-kc clock pulse generator, and data/ready inverters.

a. T-Pulse Generator. The T-pulse generator consists of an emitter follower (Q1) and a shaper (Q2) to process the T-pulse command pulse, a bistable multivibrator (flip-flop) used to halve the frequency of the shaper output, and a blocking oscillator used to generate the negative going 750-pps T-pulses.

(1) *Emitter follower Q1 and shaper Q2.* Emitter follower Q1 current-amplifies the 1,500-cps T-pulse command signal which is supplied to its base. The output of Q1, which appears across emitter load resistor R1, is used to drive the base of shaper Q2. Shaper Q2 alternates between cutoff and saturation while amplifying the signal and thus causes the collector voltage to vary between −12 volts and 0 volt respectively, at a 1,500-cps rate. The output of Q2 is an inverted and shaped replica of its input.

(2) *Multivibrator Q3, Q4.* Assume that Q3 is initially saturated and Q4 is cut off. When the output of shaper Q2 switches from −12 volts to 0 volt, gating diode CR2 becomes forward-biased, clamping the junction of current-limiting resistor R10 and blocking capacitor C4 to ground potential (0 volt). This positive-going transient is coupled through C4 to the base of Q3, which reduces the conduction of Q3 and thus results in an increased (more negative) collector voltage. Transistor Q3 collector load resistor R4, Q4 base current-limiting resistor R5, and resistor R7 form a voltage-divider network which allows a portion of the voltage change at the collector of Q3 to be coupled to the base of Q4. Capacitor C1 allows a speedier changeover by instantly applying the voltage change at the collector of Q3 to the base of Q4. Negative voltage at the base of Q4 forward-biases its base-emitter junction and causes collector current to flow. Increasing collector current causes the voltage at the collector of Q4 to drop to zero. Transistor Q4 collector load resistor R8, Q3 base current-limiting resistor R9, and resistor R6 form a voltage divider which allows a portion of the voltage change at the collector of Q4 to be coupled to the

base of Q3. This positive-going voltage further decreases Q3 collector current. This action continues until Q3 is entirely cut off and Q4 is saturated. The next time the output of Q2 switches from −12 volts to 0 volt, gating diode CR1 is forward-biased and Q4 is driven to cutoff.

(3) *Blocking oscillator Q5.* The positive transient, which occurs when multivibrator transistor Q4 goes from cutoff to saturation, is changed into a positive-going pulse by differentiator network C5, R11, and applied to the base of transistor Q5. Transistor Q5 subsequently begins to conduct and causes current to flow through the primary of transformer T1. Current induced in the secondary (pins 5 and 6) winding of transformer T1, which is caused by the increasing current flow in the primary winding, flows through current-limiting resistor R12 and through the base-emitter junction of Q5. The additional base current results in increased current flow through the primary of T1. This regenerative action continues until Q5 is saturated. At this time, current ceases to flow in the secondary winding of T1 and the base-emitter junction of Q5. Transistor Q5 is thus cut off, inhibiting current flow in the primary winding of T1. The electromagnetic field around the core of T1, which was established by current flow through the primary winding, now collapses. The collapsing field induces a voltage pulse in the secondary (pins 3 and 4) winding of T1 which is the output of this circuit (750-pps T-pulses). The negative-going 750-pps T-pulses are referenced to −12 volts for FSM or to dc ground for PCM when these signals are applied to the mode control input to this assembly. Resistor R14 is a load resistor which is used to damp ringing of the output pulse. Diode CR3 suppresses voltage spikes which tend to appear across the primary of T1 during field collapse and thus protects transistor Q5 from possible damage. Power for the blocking oscillator is supplied by Zener-diode regulated supply consisting of resistor R13, capacitor C6 and Zener diode CR4. The output of this supply is −5 volts regulated.

b. Clock Pulse Generator, 6 Kc. The 6-kc clock pulse generator consists of a blocking oscillator (Q6), an emitter follower (Q8), and an inverter (Q7). This circuit receives 6-kc square wave signals and generates 6-kc positive and 6-kc negative clock pulses.

(1) *Blocking oscillator Q6.* The operation of blocking oscillator Q6 is the same as that of Q5 described in *a*(3) above, except the secondary winding of T2 (pins 3 and 4) is not referenced by the mode control input to this assembly. Transmitter Q6 routes negative input pulses to pin $\overline{A}$ which become 6-kc negative clock pulses and to inverter Q7 which are further processed and become 6-kc positive clock pulses. The chart below identifies corresponding components:

Blocking oscillator Q5	Blocking oscillator Q6
C5	C7
R11	R15
R12	R16
Q5	Q6
CR3	CR5
T1	T2
R14	R18
R13	R17
CR4	CR6
C6	C8

(2) *Inverter Q7.* The output of Q7 therefore shifts between a 0-volt and −14-volt level and is applied to emitter follower Q8. The output of Q7 is an inverted and shaped replica of its input. The negative output pulses of blocking oscillator Q6 are coupled through Q7 base current-limiting resistor R19 to the base of Q7. These negative pulses forward-bias the base-emitter junction of Q7 and causes collector current to flow; this action reduces the collector voltage to 0 volt.

When no negative pulses are present, Q7 is held cutoff by +12 volts coupled to its base by bias resistor R20. When Q7 is cut off, its collector voltage is held to −14 volts by the voltage divider consisting of R21 and R22.

(3) *Emitter follower Q8.* This emitter follower is normally cut off by −14 volts from inverter Q7 on its base and −12 volts from the voltage divider formed by R23 and CR7 on its emitter. When inverter Q7 conducts, the base voltage of emitter follower Q8 heads toward 0 volt and causes Q8 to conduct. Current flow through emitter load resistor R23 causes the emitter voltage to drop to about 0 volt which reverse-biases clamping diode CR7. The output of emitter follower Q8 consists of positive-going pulses, 12 volts in amplitude, referenced to −12 volts.

c. Data, Ready Inverters Q9 and Q10. Data and ready inverters Q9 and Q10 invert and reshape the data and ready control signals. Data transmitter (the data control signal from the transmitter) is coupled through Q9 base current-limiting resistor R24 to the base of Q9. The data transmitter signal is a square wave varying between 0 and −15 volts. When data transmitter signal is 0 volt, the base-emitter junction of Q9 is reverse-biased by +12 volts coupled to the base through bias resistor R25. When data transmitter signal goes to −15 volts, the base-emitter junction of Q9 is forward-biased and causes collector current to flow. Current flowing through collector resistor R26 drops the collector voltage to 0 volt, which reverse-biases clamping diode CR8. When Q9 is cut off, its collector voltage is clamped to −12 volts by clamping diode CR8; thus the output of this inverter is limited to 0 volt or −12 volts. Inverter Q10 is identical. The chart below identifies corresponding components:

Inverter Q9	Inverter Q10
R24	R27
R25	R28
Q9	Q10
R26	R29
CR8	CR9

56. Frequency Divider, 1518494

(fig. 29)

The frequency divider consists of five identical bistable multivibrators (flip-flops), and a two-stage (Q11, Q12) dc isolation amplifier. The five flip-flops reduce the frequency of the square wave input by a factor of 32. The output of the last flip-flop is processed by a two-stage isolation amplifier before leaving this assembly.

a. Flip-Flop Q1, Q2. The 48-kc input to this assembly is applied to a differentiator network consisting of coupling capacitor C1 and resistor R2. The differentiator produces positive and negative spikes which are referenced to −12 volts by resistor R2 and applied to the anodes of clock-pulse gating diodes CR1 and CR2. Assume that Q1 is initially conducting and that Q2 is cut off. The positive-going spikes forward-bias CR1 and are coupled through base current-limiting resistor R4 and speedup capacitor C2 to the base of transistor Q1. The base-emitter junction of Q1 is reverse-biased by the positive spikes and subsequently ceases conducting and causes the collector voltage to rise toward −12 volts. Transistor Q1 collector load R3, Q2 base current-limiting resistor R5, and resistor R7 form a voltage divider which allows a portion of the voltage change at the collector of Q1 to be coupled to the base of Q2. Speedup capacitor C3 applies this change direct to the base of Q2. Negative voltage at the base of Q2 forward-biases its base-emitter junction and allows collector current to flow. Increasing collector current causes the voltage at the collector of Q2 to drop to 0 volt. Transistor Q2 collector load R1, Q1 base current-limiting resistor R4, and resistor R6 form a voltage divider which allows a portion of the voltage change at the collector of Q2 to be coupled to the base of Q1. Capacitor C2 is the speedup capacitor for Q1. Positive voltage on the base of Q1 further decreases its collector current. This action continues until Q1 is cut off and Q2 is saturated. During Q1 cutoff, the voltage at its collector goes to −9 volts, but does not reach −12 volts because of voltage divider R3, R5 and the base-emitter junction of Q2. When the next positive pulse appears at the anodes of CR1 and CR2, CR2 is forward-biased and initiates an action similar to that described above, but to cut off Q2 and saturate Q1.

b. Flip-Flops Q3 Q4, Q5 Q6, Q7 Q8, and Q9 Q10. Each of the four other flip-flops on this card is similar to the flip-flop described in *a* above. The following chart indicates the corresponding components:

Flip-flop Q1, Q2	Flip-flop Q3, Q4	Flip-flop Q5, Q6	Flip-flop Q7, Q8	Flip-flop Q9, Q10
R1	R8	R15	R22	R29
R2	R9	R16	R23	R30
R3	R10	R17	R24	R31
CR1	CR3	CR5	CR7	CR9
CR2	CR4	CR6	CR8	CR10
C2	C5	C8	C11	C14
C3	C6	C9	C12	C15
R4	R11	R18	R25	R32
R5	R12	R19	R26	R33
R6	R13	R20	R27	R34
R7	R14	R21	R28	R35
C1	C4	C7	C10	C13

c. Dc/Isolation Amplifier Q11, Q12. The collector voltage of transistor Q9, which varies between −9 volts and 0 volt at a 1,500-cps rate, is coupled through base current-limiting resistor R36 to the base of Q11. When the collector voltage of Q9 is at 0 volt, bias resistor R39 supplies a positive bias to the base of Q10 and holds it cutoff. The emitter voltage of Q11 is controlled at this time by current flow through transistor Q12. The base of Q12 is biased slightly negative by the voltage divider consisting of resistor R41 and diode CR11. The emitter of Q12 is thus placed at a potential of about 0 volt. Transistor Q12 collector current flowing through collector load resistor R38 establishes a collector voltage of about −2.5 volts. When the collector voltage of transistor Q9 changes to −9 volts, the base voltage of Q11 rises to about −6.5 volts. Increased current flow through common emitter resistor R40 causes the common emitters of Q11 and Q12 to be placed at a potential of about −6.5 volts, which reverse-biases the base-emitter junction of Q12. Transistor Q12 ceases to conduct and its collector voltage rises to −12 volts; thus, the output of Q12 switches between approximately −2.5 volts and −12 volts at the rate of 1,500 cps.

57. Variable Gain Amplifier and Transmitter Relay Card, 1522312

(fig. 31)

a. General. The variable gain amplifier and transmitter relay card consists of switch Q1, emitter follower Q2 and amplifier Q3, TRANSMITTER FSM/PCM selector switch S1 and relays K1, K2, K3, and K4. When TRANSMITTER FSM/PCM S1 is set to PCM, amplifier Q3 amplifies the 1,500-cps signal output of the bandpass filter on assembly 1518484 (para. 54). Resistor R4, in the emitter circuit of Q1, is the termination resistor for that filter; it is connected with the filter through relay K2. Switch S1 sets relays K1 through K4 to their relative positions for either FSM or PCM transmitter operation.

b. Operation. Transistor switch Q1 switches the 1,500-cps signal in or out (modulated) with the data transmitter, data control signal, from the output buffer. The data transmitter signal is a square wave varying between 0 and −15 volts. Current-limiting resistor R1 and bias resistor R2 control the incoming logic levels of 0 volt and −15 volts to approximately +5 volts and −7.2 volts respectively. A −7.2-volt signal applied to the base of switch Q1 causes Q1 to conduct. This prevents the 1,500-cps filter output signal from appearing at the base of Q2. A +5-volt signal applied to the base of switch Q1 cuts off Q1 and allows the 1,500-cps signal to pass to the base of Q2, via level control potentiometer R5, and relay K2 when switch S1 is set to PCM. The signal input across R4 is a sine wave approximately 6.5 volts peak-to-peak. Potentiometer R5, in the base circuit of Q2, provides an adjustment of the input signal amplitude. Approximately 12 percent of the signal appears across isolation resistor R3, which leaves about 88 percent or 5.7 volts peak-to-peak available for adjustment across R5. Resistor R3 isolates the signal source from ground when Q1 is saturated. Voltage-divider resistors R6 and R8 establish an approximate +7.2-volt level at the collector of emitter follower Q2. Capacitor C3 is a filter capacitor. About 1 ma of current flows in the base circuit of amplifier Q3, providing a possible gain of 10. The voltage established at the junction of R10 and R11 is alternating current (ac) grounded by emitter bypass capacitors C4 and C5. The capacitors prevent any of the 1,500-cps

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signal from appearing across R11. Resistor R11 serves as a current limiter without reducing the ac signal gain of the amplifier. Only slight degeneration occurs through the small resistance of R10. The amplitude of this signal then becomes the product of the voltage applied, the gain obtained, and the ratio of the collector resistance (R9) to the total resistance of the output circuit. The amplified signal appears across collector load resistor R9 and is ac coupled through coupling capacitor C6. Resistor R12 provides isolation between the amplifier output and the 600-ohm line driver on 549591 (para. 52).

c. Level Shifter R13 and R14. The level shifter receives a 1,500-cps square wave signal from frequency divider 1518494 (para. 56). This signal is level shifted by the +27-volt regulated supply and level shifting resistors R13 and R14 to provide the proper triggering level for the T-pulse generator 1518493 (para. 55).

Section II. RECEIVER SUBFUNCTION

58. Data Input Filter and First Limiter Amplifier, 1518324

(fig. 15)

a. General. The data input filter and first limiter amplifier consists of the data input circuit and the first limiter amplifier circuit. The data input filter and first limiter amplifier receives the input FSM message, amplifies this message and routes it to the second limiter amplifier and frequency discriminator 1518326.

b. Data Input Circuit. The data input circuit consists of an input transformer and T-pad attenuator, surge diodes CR1 and CR2, and bandpass filter FL1.

(1) *Input transformer and T-pad attenuator.* Input transformer T1 is a 600-ohm input isolation transformer with a turns ratio of 1 to 1. The secondary of transformer T1 is connected to a T-pad consisting of resistors R1, R2, and R3 which attenuate the input to filter FL1 by approximately 6 db.

(2) *Surge diodes CR1 and CR2.* Surge limiting Zener diodes CR1 and CR2 are located between the attenuator T-pad and the bandpass filter. These two Zener diodes limit the voltage that appears at the input terminal of the bandpass filter to a maximum of ±12 volts. The two Zener diodes are connected back-to-back across the T-pad output. Thus, any large voltage on the output of the T-pad will be directed through the Zener diodes to ground. This prevents a surge in line voltage and protects the bandpass filter and components in subsequent circuits from damage. The breakdown voltage of both diodes is 12 volts.

(3) *Bandpass filter FL1.* The bandpass filter is a sealed unit, which receives its input direct from the T-pad. This filter attenuates all frequencies above and below the frequencies of the FSM message frame; therefore, noise and interference have a minimum effect on circuits following the bandpass filter. The output of FL1 is applied to the first limiter amplifier.

c. First Limiter Amplifier Circuit. The first limiter amplifier circuit consists of an amplifier circuit, a feedback circuit, and two filter circuits. The first limiter amplifier amplifies the input FSM message and provides limiting action such that the output is not greater than ±3.1 volts. Decoupling circuits are also provided for the ±12-volt supply voltages because of the critical bias requirements of many circuits making use of these supply voltages.

(1) *Amplifier circuit.* The amplifier circuit consists of differential amplifier Q1, Q2, emitter follower Q3, inverter Q4, and emitter follower Q5. The signal from bandpass filter FL1 is applied through input resistor R6 to the base of Q1. Transistor Q1 provides circuit isolation between the data input circuits and succeeding transistor stages of the first limiter amplifier. The differential amplifier is used here as a straightforward dc voltage amplifier. Its output of R7 is of the same polarity as its input at the base of Q1. In a static condition, the emitter-base junctions of Q1 and Q2 are forward-biased as a result of the +12-

volt filter supply in the emitter circuit. The signal is amplified by Q2 and the output of Q2 is developed across collector load resistor R7 and applied through R11 to the base of emitter follower Q3. The output of Q3 is developed across emitter load resistor R12, is in the same phase as its input, and is applied to the base of inverter Q4. Clamping diode CR3 is a Zener diode which clamps the emitter of Q4 at −5.6 volts. The path for reverse-bias current CR3 is through current-limiting resistor R14 to the +12-volt supply. The biasing circuit of CR3 and R14 provides a stable bias for Q4 and a low impedance to the signal. This condition eliminates any degenerative feedback and results in a stable voltage amplifier with very high gain. The signal, inverted by Q4 to provide the correct phase signal to the feedback circuits, is developed across load resistor R13 and applied to the base of emitter follower Q5. Emitter follower Q5 does not invert the signal and provides a low impedance output from the first limiter amplifier for correct impedance matching to the second limiter amplifier (para. 59). Its output is also routed to feedback limiters Q6, Q7, 180° out of phase with the signal at the input to Q1 of the differential amplifier (input to amplifier circuit). Resistor R15 is an emitter load resistor for Q5, and resistor R23 is a current-limiting collector resistor for Q5. The network composed of capacitors C5, C4, and C3 and resistors R9 and R11 is a frequency and phase shift compensating circuit that allows equal amplification for all signal frequencies and puts the feedback signal in correct time relationship with the input signal so that cancellation can take place. The feedback circuit limits the swing of the amplifier circuit such that the output at TP2 varies within ±3.1 volts.

(2) *Feedback circuit.* The feedback circuit consists of feedback limiters Q6 and Q7, a dc bias network consisting of resistors R16, R17, and R18, and filter capacitor C6. The feedback circuit provides degenerative feedback to the amplifier circuit and dc bias stabilization between the input and output stages. The feedback limiters function only when the amplifier output exceeds ±3.1 volts. When the amplifier circuit output is within these limits, feedback limiters Q6 and Q7 are cut off. Dc bias for the base of Q1 is developed from the emitter voltage of Q5. The emitter voltage from Q5 is applied through R17 to C6; R16, R17 and C6 act as a low-pass filter which charges to approximately the average voltage at the emitter of Q5. This average voltage is applied through R16 to the base of Q1. Resistors R24 and R25 are current-limiting collector resistors for protection of Q6 and Q7.

(*a*) *Large negative output.* When the amplifier output is more negative than −3.1 volts, the voltage developed across voltage divider R21 and R22 causes the base of Q7 to go negative. A negative voltage at the base of Q7 reverse-biases Q7 and it remains at cutoff. At the same time, the voltage developed across voltage divider R19 and R20 causes the base of Q6 to go negative. A negative voltage at the base of Q6 forward-biases Q6 and causes it to conduct; this action allows a negative voltage to be developed on the emitter. This negative emitter voltage is combined with the positive portion of the input signal to lower the amplitude of the voltage at the base of Q1 and therefore limit the amplifier output to −3.1 volts.

(*b*) *Large positive output.* When the amplifier output is more positive than +3.1 volts, a positive voltage is applied to the bases of Q6 and Q7. Transistor Q6 becomes reverse-biased and remains cut off, and Q7 becomes forward-biased and conducts. With Q7 conducting, a positive voltage is developed on the emitter. The positive emitter voltage is combined with the negative input signal to limit the voltage at the base of Q1. This input voltage lowers the amplifier output to +3.1 volts.

(c) *Filter circuit.* To isolate the first limiter amplifier from the biasing supplies, the +12-volt and the −12-volt supply voltages are routed through the decoupling filter circuits before being applied to the transistors in the first limiter amplifier. The filter circuit for the +12-volt supply consists of isolation resistor R4 and filter capacitor C1. The filter circuit for the −12-volt supply consists of isolation resistor R5 and filter capacitor C2. The first limiter amplifier loads the filter circuits so that a dc voltage drop of approximately 0.8 volt occurs across R4 and R5. The resulting filter voltage is 11.2 volts.

59. Second Limiter Amplifier and Frequency Discriminator, 1518326

(fig. 16)

a. General. The second limiter amplifier and frequency discriminator consists of a second limiter amplifier circuit, a squaring amplifier circuit, and a frequency discriminator circuit. The input to the second limiter amplifier and frequency discriminator (from the first limiter amplifier circuit 1518324) is a sine wave normally clipped at ±3.1 volts, but possibly too small to be clipped.

b. Second Limiter Amplifier. The second limiter amplifier is similar to the first limiter amplifier (para. 58) except that some component values differ from the values of corresponding components in the first limiter amplifier. (See the chart below.) The second limiter amplifier amplifies and shapes the signal. The amplifier output is a ±3.5-volt (TP2) square wave. The second limiter amplifier consists of differential amplifier Q6, Q7, emitter follower Q8, inverter Q9, emitter follower Q10, and feedback limiters Q4, Q5. The input signal is supplied through coupling capacitor C3 and input resistor R7 to the base of Q6. Capacitor C3 and resistor R7 isolate the first limiter amplifier from the second limiter amplifier. Output-signal limiting is provided by feedback limiters Q4 and Q5 which are identical in operation to the feedback limiters in the first limiter amplifier. Similarly, the biasing network comprising resistors R13, R14, and capacitor C5 serve the same purpose as resistors R16 and R17 and capacitor C6 in the first limiter amplifier. The output of the second limiter amplifier is routed to the squaring amplifier circuit.

First limiter amplifier element	Second limiter amplifier equivalent element
Q1–Q5	Q6–Q10
R6, 619 ohms	R7, 1,210 ohms
R8	R16
R7	R15
R10, 620 ohms	R18, 1,200 ohms
R9	R17
C3	C4
R11	R19
C4	C6
C5	C7
R14	R21
R12	R20
R13	R22
R15	R24
R23	R33
CR3	CR1
Q6–Q7	Q4–Q5
R24–R25	R52–R53
R19–R22	R8–R11
R18, 61.9K ohms	R12, 215K ohms
R16, 3,320 ohms	R13, 3,300 ohms
R17, 4,750 ohms	R14, 4,700 ohms
C6, 3 μf	C5, 34μf

c. Squaring Amplifier Circuit. The squaring amplifier circuit consists of amplifier Q1, amplifier Q2, and emitter follower Q3. The input to the squaring amplifier circuit is a sine wave (normally clipped at ±3.5 volts, but possibly too small to be clipped) received from the second limiter amplifier circuit.

(1) *Positive-going input.* Assume that the positive-going edge of the square wave is being applied through input resistor R3 to the base of amplifier Q1. Transistor Q1 becomes reverse-biased and current flow through collector resistor R1 to the emitter of Q1 begins to decrease. With less voltage drop across R1, the collector potential of Q1 increases toward −12 volts. The negative-going change in potential is applied to the base of amplifier Q2 through coupling capacitor C1 and input resistor

R4. A negative voltage at the base of Q2 forward-biases Q2 and causes an increase in current flow through collector load resistor R6. An increased voltage drop across R6 causes the voltage at the collector of Q2 and the base of emitter follower Q3 to approach 0 volt. A part of this positive-going voltage is fed back through R2 to the input of Q1. The feedback voltage adds to the input signal and allows Q1 to be cut off more rapidly. This increases the net gain and reduces the net switching time of Q1, Q2. A 0-volt signal at the base of Q3 reduces the forward-bias and the current flow through collector load resistor R51, transistor Q3, and emitter load resistor R25. A volt level at the base of Q3 causes the voltage at the emitter of Q3 to rise to approximately 0 volt. The positive-going emitter voltage, coupled through feedback capacitor C2 develops a sharp, positive pulse at the base of Q1. The feedback voltage further decreases the time required to cut off Q1 and shortens the risetime of the voltage at the output of Q3.

(2) *Negative-going output.* Assume that the negative-going edge of the square wave is being applied through input resistor R3 to the base of amplifier Q1. Amplifier Q1 becomes forward-biased and causes an increase in the current flow through collector load resistor R1. With an increased voltage drop across R1, the collector of Q1 rises toward 0 volt. The positive-going change in collector potential is applied to the base of amplifier Q2 through coupling capacitor C1 and resistor R4. A positive voltage at the base of Q2 reverse-biases Q2 and decreases current flow from the −12-volt supply through collector load resistor R6. A decreased voltage drop across R6 causes the voltage at the collector of Q2 and the base of emitter follower Q3 to increase toward −12 volts. A part of this negative voltage is fed back through R2 to the input of Q1. A negative voltage at the base of Q3 increases the forward-bias of Q3 and thus increases the current flow through emitter load resistor R25. The increase in current flow through R25 causes a negative voltage to be fed back through capacitor C2 to the base of Q1.

(3) *Output circuit.* The output of Q3 is a square wave that varies between 0 and −7.5 volts and can be seen at TP1. Emitter follower Q3 drives two differentiating circuits, C10, R37, R39 and C8, R26. The pulses from C8 and the output of Q13 are applied to the base of Q11 which inverts the combined signal. Pulses from C10 and the output of Q14 are supplied to FL1.

d. Frequency Discriminator Circuit.

(1) *General.* The frequency discriminator consists of two one-shot multivibrators Q11, Q12 and Q14, Q15; three emitter followers Q13, Q16, and Q17; an and gate CR6, CR11 and R48; resistor-capacitor filter FL1; a diode-resistor isolation network; and a low-pass filter. The diode-resistor isolation network and low-pass filter are contained in data logic amplifier 1518327 and are discussed in paragraph 60. The inputs to the frequency discriminator are positive and negative pulses at the frequency of the FSM message. The output of the frequency discriminator portion of this card is applied to the data logic amplifier circuit (1518327) and is shown on figure 8.

(2) *One-shot multivibrator Q14, Q15, and emitter follower Q16.* When the voltage at the output of the squaring amplifier decreases from −7.5 volts to 0 volt, a short positive pulse is developed at the anode of steering diode CR8 because of the differentiating action of capacitor C10 and resistors R37 and R39. The anode of CR8 is normally negative with respect to the cathode due to −6.5 volts at the junction of voltage divider R37 and R39 and −6 volts at the junction of voltage divider R42 and R43. The positive pulse applied to the anode of CR8 forward-biases CR8 and a positive pulse is applied to terminal 4 of filter FL1. Filter FL1 contains a capacitor connected between terminals 4 and 1 and a resistor

connected between terminals 3 and 1. Terminal 3 is also connected to the −12-volt supply. The negative supply voltage normally keeps inverter Q15 conducting and results in approximately +11 volts at terminal 1. The incoming positive pulse applied to terminal 4 is coupled through the capacitor of FL1 to terminal 1 and to the base of Q15. This short, positive pulse at the base of Q15 reverse-biases Q15 and cuts it off. When Q15 is cut off, −12 volts is applied through R46 to the base of emitter follower Q16. Emitter follower Q16 conducts through emitter load resistor R47, through or gate CR11 and R48 and the base of $\overline{Q17}$, and through the base of Q14 through a coupling network consisting of surge-limiting resistor R45, current-limiting resistor R44, and speed-up capacitor C11. The voltage at the emitter of Q16 is approximately −11 volts during conduction. The voltage divider consisting of CR7 and R41 holds the emitter of Q14 at +5.6 volts when Q16 is cut off. However, when Q16 is conducting, Q14 is saturated and the emitter voltage is approximately +5 volts. The collector current of Q14 flows through bias resistor R38, clamp CR10 or gate R42 and CR9 and through collector load resistor R40; this action causes the voltage at the anodes of CR9 and CR10 to be approximately +0.5 volts and holds terminal 4 of FL1 at approximately 0 volt. Transistor Q15 remains reverse-biased until the capacitor between terminals 1 and 4 of FL1 discharges through the internal resistance of FL1 a sufficient amount to lower the base of Q15 to less than +12 volts. The time required is 260 microseconds. When the base of Q15 goes negative with respect to the emitter, Q15 becomes forward-biased and conducts; this action causes current flow through R46. The voltage drop across R46 causes the potential at the collector of Q15 and the base of Q16 to go positive. The positive voltage reverse-biases Q16 and current flow through R47 ceases. The output of Q16 goes to +12 volts which reverse-biases Q14 and CR11. When Q14 is cut off, the voltage at the junction of CR9 and CR10 is −12 volts. Only the positive-going edge of the square wave triggers the multivibrator circuit. When the incoming square wave goes from 0 volt to −7.5 volts, a negative pulse is developed at the anode of CR8, and CR8 remains reverse-biased. The output of the multivibrator is a negative-going pulse with a width of 260 microseconds and a repetition rate equal to the carrier frequency of the applied FSM message. When the input frequency is 1,125 cps, the output is negative for 260 out of 888 microseconds. When the input is 1,500 cps, the output is negative for 260 out of 667 microseconds. When the input is 1,875 cps, the output is negative for 260 out of 533 microseconds. The negative-going pulse output is applied through an or gate to emitter follower Q17.

(3) *One-shot multivibrator Q11, Q12 and emitter follower Q13.* Multivibrator Q11, Q12 and emitter follower Q13 are similar to multivibrator Q14, Q15 and emitter follower Q16 except for the input circuit. When the voltage level at the squaring amplifier increases from 0 to −7.5 volts, a negative pulse is developed across C8 and passed by steering diode CR3 to the base of Q11, inverted, and then applied to filter FL1. The output of this circuit is a negative pulse with a width of 260 microseconds and a repetition rate equal to the carrier frequency of the incoming FSM message.

(4) *Multivibrator output circuit.* The outputs of the two multivibrator emitter followers (Q13 and Q16) are applied to a negative or gate composed of CR6, CR11, and R48. Each time a negative pulse is developed at the output of one of the multivibrators, the negative pulse is passed through the negative or gate to the base of emitter follower Q17. The negative voltage increases the forward-bias of Q17 and causes an increase in the current through collector resistor R49, transistor Q17,

and emitter resistor R50 which provides a ±3.5-volt output. An increase in the voltage drop across R50 causes the emitter potential to go negative and produces a −10-volt output. Since the output of Q17 is negative when either one-shot multivibrator is negative, the signal on TP3 is a square wave train negative for 260 microseconds and positive for 184 microseconds for a 1,125-cps input, a train of positive 73-microsecond pulses for a 1,500-cps input, and a train of positive 6-microsecond pulses for a 1,875-cps input. Positive pulses are always separated by 260 microseconds.

60. Data Logic Amplifier, 1518327

(fig. 17)

a. General. The data logic amplifier contains the remaining portion of the frequency discriminator (major portion contained in the second limiter amplifier and frequency discriminator 1518326, para. 59), a data detector circuit, and a base-band data limiter amplifier.

b. Frequency Discriminator. The remaining portion of the frequency discriminator consists of a diode-resistor isolation network and low-pass filter FL1. The input to this network is either −10 volts or +3.5 volts. When the input is +3.5 volts, current flows through all four diodes. The voltage drop across these diodes causes the anodes of CR1 and CR2 to be placed at a potential of about +3.7 volts and the cathodes of CR3 and CR4 at a potential of about −3.3 volts. The total voltage across the series combination of CR2 and CR4 is now about 0.4 volt. Assuming equal voltage drops across CR2 and CR4, the output of the network is about +3.5 volts. When the input changes from +3.5 volts to −10 volts, the input to filter FL1, which is capacitive, begins to discharge. At this time, CR1 and CR4 are conducting and CR2 and CR3 are reverse-biased. The anodes of CR1 and CR2 are at a potential of about −9.8 volts and the cathodes of CR3 and CR4 at a potential of about +3.3 volts (provided the input to the filter is still at a potential of about +3.5 volts). The input to the filter discharges through CR4 and R2 until it reaches a potential of 0 volt and then charges toward −6 volts through the same path. When the input is −10 volts, CR2 is reverse-biased and the maximum voltage to which the filter input may charge (−6 volts) is determined by a voltage divider consisting of CR4, FL1, and resistors R2 through R8. When the input to the network again goes to +3.5 volts, the input to the filter begins to discharge through CR2 and R1. This action places the anodes of CR1 and CR2 at potential of about −5.8 volts, reverse-biasing CR1. CR3 conducts and places a potential of +3.3 volts on the cathodes of CR3, CR4 which reverse-biases CR4. Diodes CR1 and CR4 remain reverse-biased until the input again goes to −10 volts. During a positive-going pulse, the input to the filter charges to a potential which is determined by the time that the input remained at a potential of +3.5 volts. When space frequency signals are being received, the input remains at +3.5 volts for about 6 microseconds to allow the filter input to reach a potential of about −3 volts. When ready frequency signals are being received, the input remains at +3.5 volts for 73 microseconds and the filter input reaches a potential of about 0 volt. When mark frequency signals are being received, the input remains at +3.5 volts for 184 microseconds and the filter input reaches a potential of about +3 volts; thus, changes in frequency are converted to changes in amplitude. Filter FL1 attenuates those portions of the diode-resistor network output signal having a frequency greater than 540 cps.

c. Base-Band Data Limiter Amplifier. The base-band data limiter amplifier is similar to the first limiter amplifier (para. 58) except that feedback limiters Q6, Q7, limit the output signal at the emitter of Q5 to a maximum of ±7.5 volts, there is no speedup capacitor between the collector of Q2 and the base of Q3, and the base bias of Q1 is not controlled by Q5. The chart below lists the elements of the first limiter amplifier and their equivalent elements in the base-band data amplifier. The gain of the amplifier, as determined by feedback resistor R21 and input resistor R4, is 16.5 db. Voltage level control R6 is adjusted so that the current flow through resistors R4 through R8 provides a 0-volt dc level at the base of Q1 during the ready frequency of the FSM message. Hence, mark frequency is a positive voltage, and space frequency is a negative voltage at the base of Q1. The output of the amplifier is called BBD (base-band data). The 0-volt level at the output represents ready frequency in the FSM message,

the +7.5-volt level represents space frequency in the FSM message, and the −7.5-volt level represents mark frequency in the FSM message. The BBD output is routed to the 1,500-cps detector 1518325 (para. 61).

First limiter amplifier element	BBD amplifier equivalent element
Q1–Q7	Q1–Q7
R6, 619 ohms	R4, 1,780 ohms
R8	R9
R7	R10
R10, 620 ohms	R13, 1,800
R9	R11
C3	C1
R11	R12
R12	R14
R13	R16
C5, 220$\mu\mu$f	C2, 680$\mu\mu$f
R14	R15
R23	R17
R15	R18
CR3	CR5
R24–R25	R43–R44
R19, 3,830 ohms	R19, 3,160 ohms
R20, 1,000 ohms	R20, 1,960 ohms
R22, 3,830 ohms	R23, 3,160 ohms
R21, 1,000 ohms	R22, 1,960 ohms
R18, 61.9K ohms	R21, 12.1K ohms

d. Data Detector Circuit. The data detector circuit detects the BBD output from Q5 (*c* above). The BBD signal can be one of three levels for an incoming message: 0 volt for ready frequencies, positive (+7.5 volts maximum) for space frequencies, and negative (−7.5 volts maximum) for mark frequencies. The operation of the data detector circuit (Q8–Q13) is identical when either a ready or space frequency is present in the incoming message. With 0 volt or positive input to Q8, the output of Q12 ($\overline{\text{data}}$) is 0 volt and the output of Q13 (data) is −15.5 volts (−12 volts when an external load is connected to Q13 at pin E). The output of Q12 is −6 volts and the output of Q13 is 0 volt when the input to Q8 is negative. When the base input to Q8 is positive, Q8 is cut off and Q9 is saturated; the reverse is true when the base input to Q8 is negative. The collector resistors for Q8 and Q9 are R25 and R28 respectively. Resistor R26 is a base current-limiting resistor, and C3 is a speedup capacitor. Resistor R27 and the +12-volt supply at the base of Q9 provides the cutoff bias for Q9. Resistor R24 is a base current-limiting resistor for Q8. The output of emitter follower Q10 is positive when Q9 is saturated and is negative when Q9 is cut off. Resistor R29 and capacitor C4 form a regenerative feedback network which increases the switching action of Q8–Q10. Resistor R30 is the load resistor for emitter follower Q10. Resistor R31 at the collector of Q10 is a current-limiting resistor. The output of Q10 is fed to Q11 and Q13. The output of Q13 is data, and the output of Q11 is fed to Q12 which provides the data output.

(1) *Data output.* When the output of Q10 is positive (ready or space frequency present), the output of Q13 is −15.5 volts (−12 volts when an external load is connected to Q13 at pin E). The Q13 output is 0 volt when the output of Q10 is negative (mark frequency present). Resistor R38 is a base current-limiting resistor, and R39 and the +12-volt supply provide cutoff bias for Q13. Resistor R40 is the collector resistor for Q13. Capacitor resistor CR7, resistor R41, and the −12-volt supply at the collector of Q13 clamps the output to a negative level when Q13 is cut off. Resistor R42 is a current-limiting resistor connected from the collector of Q13 to the pin H output (not used). Data is available at pin E.

(2) *$\overline{\text{Data}}$ output.* When the output of Q10 is negative (mark frequency present), Q11 is saturated and Q12 is cut off; the reverse is true when the Q10 output is positive (space or mark frequency present). The data output is −6 volts when Q12 is cut off and the data output is 0 volt when Q12 is saturated. The +12-volt supply and R32 provide cutoff bias for Q11. The base current-limiting resistors for Q11 and Q12 are R33 and R35, respectively. Capacitor C5 is a speedup capacitor. The collector resistors for Q11 and Q12 are R34 and R37, respectively. Resistor R36 and the +12-volt supply provide cutoff bias for Q12.

Diode CR6 clamps the input of Q12 to −6 volts when Q12 is cut off.

61. Detector, 1,500 Cps, 1518325

(fig. 18)

a. General. The 1,500-cps detector consists of a mark detector circuit, a space detector circuit, and a midfrequency component (MFC) detector circuit. The input to the 1,500-cps detector is base-band data (BBD) which consists of ready, mark, and space voltage levels. The space voltage is the most positive level (+7.5 volts), ready is the intermediate level (0 volt), and mark is the negative level (−7.5 volts). These voltages may be observed at TP1.

b. Mark Detector Circuit. The mark detector circuit consists of mark detector flip-flop Q1, Q2 and inverter Q13. The input signal to the detector is applied to the base of Q1 through input resistor R1. A negative input signal of at least −3 volts is necessary to bias Q1 into conduction since one end of base bias resistor R2 is connected to the +12-volt supply. When a mark voltage level (−7.5 volts) is applied to the base of Q1, current flows through collector load resistor R5. The current flow through R5 causes the collector of Q1 to go to approximately 0 volt. The positive-going voltage is applied to the base of Q2 via resistor R6 and capacitor C2. Transistor Q2 becomes reverse-biased and is cut off. With Q2 cut off, voltage from the −12-volt supply is applied to the base of Q1 to aid the incoming signal. This action shortens the switching time of Q1. The 0-volt output of the mark detector (collector voltage of Q1) develops to positive voltage at the junction of resistors R8 and R39 and this voltage is routed to the base of inverter Q13. A positive voltage at the base of Q13 reverse-biases Q13 and cuts it off. When Q13 is not conducting, no current flows through collector resistor R40, and the voltage at the collector of Q13 is −12 volts. The −12 volts from the collector circuit of Q13 is applied to the MFC nor gate Q3 and to logic converter Q9 (1522348, para. 67) as a −3-volt detector. Since only the mark voltage level is negative enough to cause Q1 to conduct, the space and ready voltage levels cause Q1 to cut off and produce a negative voltage at the collector of Q1. A negative voltage at the base of Q13 forward-biases Q13, and ground potential is developed at the collector. With the collector at ground potential, −12 volts is dropped across collector resistor R40, and the ground potential is applied to the MFC nor gate and to logic converter Q9 of 1522348.

c. Space Detector Circuit. The space detector circuit consists of space detector flip-flop Q9, Q10 and inverter Q8. The space detector flip-flop is similar to the mark detector flip-flop except that base bias resistor R24 is tied to the −12-volt supply instead of the +12-volt supply. The output of the flip-flop is taken from the collector of Q10. Since base bias resistor R24 is tied to the −12-volt supply, the base of Q9 is positive when the input signals to the detector is +3 volts or more. Only a space voltage level (+7.5 volts) can reverse-bias Q9 and cut it off. When Q9 is cut off by a space input voltage, the collector supply voltage of Q9 is applied to the base of Q10 and causes Q10 to conduct. The voltage developed across R26 causes the voltage at the collector of Q10 to go positive. Since the flip-flop output is taken at the collector of Q10, the output is in phase with the signal at the base of Q9. The mark and ready signals apply a negative voltage to the base of Q9 which, in turn, produces a negative output. The output of the space flip-flop is applied to inverter Q8. When Q10 conducts, the voltage developed across R26, R21, and R20 results in a positive voltage on the base of Q8. This positive voltage reverse-biases Q8 and cuts it off. With Q8 cut off, no current flows from the −12-volt supply through collector load resistor R22, and the potential at the collector is −12 volts. The −12-volt potential from the collector of Q8 is applied to MFC nor gate Q3 and to start/remote detector 1522348 as a +3-volt detector. A negative voltage at the base of Q8 forward-biases Q8, and ground is applied to the collector circuit. The 0-volt potential from the collector of Q8 is applied to the MFC nor gate and to the start/remote detector.

d. Midfrequency Component Detector Circuit.

(1) *General.* The MFC detector consists of nor gate Q3, low-pass filter FL1, differential amplifier Q11, Q12, switch circuit Q4, Q5, Q6, and inverter Q7. The inputs to the MFC detector are the outputs of the mark and space detector circuits.

(2) *MFC nor gate Q3.* The MFC input nor gate is similar to the nor gate discussed in TM 11-5895-264-25, except for limiting diode CR1, emitter bias resistor R11, and clamping diode CR2. With a negative voltage applied to either input resistor, R41 or R9, diode CR1 is forward-biased and the base of Q3 is slightly negative. The emitter is slightly positive because of the voltage drop across R11 and CR2. Only a small voltage change at the base of Q3 is necessary to control the conduction of Q3. The only time both inputs to Q3 are positive, and hence the output of Q3 is negative, is when a ready voltage level (0 volt) is applied to mark and space detectors. At all other times, the output of Q3 is 0 volt. The output of Q3 is routed through low-pass filter FL1 to differential amplifier transistor Q11.

(3) *Differential amplifier Q11, Q12.* The differential amplifier consisting of Q11 and Q12 exhibits nearly constant emitter potentials which occur as a result of the nearly constant current flow through common emitter resistor R34. Small variations in emitter voltage are due to the degenerative action of emitter resistors R31 and R36 and emitter balance control R33. When the voltage on the base of Q11 goes negative, due to an entering ready signal, Q11 conducts heavily, current flow through collector resistor R32 increases, and the collector potential of Q11 goes in a positive direction. With an increase in current through Q11, the potential across common emitter resistor R34 increases, forward bias for Q12 decreases, and its collector potential goes toward −12 volts. When the negative signal coming from FL1 goes sufficiently negative, Q11 saturates and Q12 cuts off.

(4) *Switching circuit Q4, Q5, and Q6.* The combination of the collector of Q11 going toward 0 volt and the collector of Q12 going toward −12 volts causes Q5 to conduct and then to saturate and causes Q4 to cut off. When Q5 conducts, its collector potential becomes negative due to the relatively large value (47 kilohms) of collector resistor R14. Negative voltage on the base of Q6 causes it to conduct, which reduces the voltage at the junction of collector resistor R15 and feedback resistor R16. This reduced (positive-going) voltage is coupled through R16 to the base of Q5 and causes Q5 to saturate, which also causes Q6 to saturate. Transistors Q5 and Q6 remain saturated until the voltage on the collector of Q11 increases negatively, and the voltage on the collector of Q12 increases positively to a value which reverse-biases the base-emitter junction of Q5; this condition drives both Q5 and Q6 into cutoff; thus, when a ready signal enters, the MFC output at Q6 is a positive-going pulse.

(5) *Inverter Q7.* The base of inverter Q7 receives the MFC signal through input resistor R17 from the collector of Q6. Base bias resistor R18 aids in establishing the base bias for Q7.

(*a*) Assume that the positive-going portion of the MFC signal is applied to the base of Q7. A positive voltage at the base of Q7 reverse-biases Q7, cuts it off, and prevents current flow through Q7 collector load R19. With no current flow through R19, the collector potential of Q7 increases in a negative direction. The output at the collector of Q7 is routed to integrator reset switch Q15 (1522348, para. 67) as $\overline{\text{MFC}}$.

(*b*) Assume that the negative-going portion of the MFC signal is applied to the base of Q7. A negative voltage applied to the base of Q7 forward-biases Q7 and causes current flow from the −12-volt supply through R19 and Q7 to ground. The voltage drop across R19 causes the collector potential of Q7 to increase in a positive direction to approximately 0 volt.

e. Circuitry Not Used. Transistor Q14 and its associated circuitry is not used.

62. IRP and DCP Generator, 593982

(fig. 19)

The IRP generator consists of an and gate

and blocking oscillator Q1. The IRP command and 6-kc negative clock pulses are anded together. When the IRP command logic is true (0-volt level) the 6-kc clock pulses are applied to the blocking oscillator which results in a 0- to −6-volt pulse output. The blocking oscillator circuit is identical with the one used in the 6-kc clock pulse generator (para. 55). The DCP generator is identical with the IRP generator, except that the 6-kc clock pulse is anded with the DCP command. When the DCP logic is true, the 6-kc clock pulse triggers the blocking oscillator; this action results in a −6-volt output pulse that is routed to the input buffer for timing purposes.

63. Synchronizer No. 1, 1518302

(fig. 22)

Synchronizer No. 1 consists of three bistable multivibrators (flip-flops) with their associated control gates and inverter Q9. Logic levels used in this assembly are −12 volts for true and 0 volt for false. The logic levels of the sync data receiver signal, at the output receiver of this assembly, are 0 volt for true and −6 volts for false. The flip-flops used in synchronizer No. 1 are similar to those used in synchronizer No. 2. Flip-flop SQ1 of synchronizer No. 2, which is typical, is described in paragraph 64.

a. Flip-Flop Gating. The operation of the input gates for all the flip-flops on this assembly is described below:

(1) $\overline{SQ4}$. Data receiver and $\overline{SQ5}$ true enable the and gate consisting of diodes CR1, $\overline{CR2}$, and pulldown resistor R8; Q1 cuts off and Q2 conducts. Signal $\overline{SQ4}$ goes true while SQ4 goes false.

(2) SQ4. $\overline{Data}$ receiver and $\overline{SQ4}$ true enable the and gate consisting of diodes CR5, $\overline{CR6}$ and pulldown resistor R10; Q2 cuts off and Q1 conducts. Signal SQ4 goes true while $\overline{SQ4}$ goes false.

(3) $\overline{SQ5}$. $\overline{Data}$/open receiver and ready/ready start receiver true enable the and gate consisting of diodes CR8, $\overline{CR9}$, CR10 and pulldown resistor R18; Q3 cuts off and Q4 conducts. Signal $\overline{SQ5}$ goes true while SQ5 goes false.

(4) SQ5. Data receiver $\overline{SQ5}$; and SQ4 true enable the and gate consisting of diodes CR12, $\overline{CR13}$, CR14 and pulldown resistor R20. When all the inputs to the and gate are true, SQ5 goes true and $\overline{SQ5}$ goes false.

(5) $\overline{SQ6}$. $\overline{Data}$ receiver and $\overline{SP2}$ true enable the and gate consisting of diodes CR25, $\overline{CR26}$ and pulldown resistor R38. Transistor Q7 cuts off and Q8 conducts. A true logic level is produced at $\overline{SQ6}$ with a false logic level at SQ6.

(6) SQ6. Data rcvr and $\overline{SP2}$ true enable the and gate consisting of diodes CR28, $\overline{CR29}$, and pulldown resistor R40. Transistor Q8 cuts off and Q7 conducts. A true logic level is produced at SQ6 with a false logic level at $\overline{SQ6}$.

b. Inverter Q9. When $\overline{SQ6}$ is true (−12 volts), the output of the voltage divider formed by R41 and R42 reverse-biases the base-emitter junction of Q9 and causes it to cease conducting. When current ceases to flow through collector load resistor R43, the collector voltage of Q9 rises toward +12 volts but is clamped to 0 volt by diode clamp CR31. When $\overline{SQ6}$ is false (Ov), Q9 is saturated and places its collector at a potential of about −6 volts; thus, $\overline{SQ6}$ is transformed from the logic levels used on this assembly to the standard system logic levels.

64. Synchronizer No. 2, 1518303

(fig. 23)

Synchronizer No. 2 consists of three identical bistable multivibrators (flip-flops) and the associated control circuits forming a module (MOD) 8 counter, a clamp (Q7) to reset the counter, and three gates (Q8, Q9 and Q10, Q11) used to generate output signals $\overline{SP2}$, IRP and DCP.

a. MOD 8 Counter. The logic levels used in this counter are −12 volts for true and 0 volt for false. The counter is clocked by 6-kc positive clock pulses which are referenced to −12 volts. The first flip-flop in the counter, SQ1, switches at a 6-kc rate. Flip-flop SQ2 switches at one-half the rate of SQ1 (3 kc), and SQ3 switches at one-half the rate of SQ2 (1.5 kc). The counter is reset by clamp Q7.

(1) *Flip-flop SQ1.* Flip-flops SQ1 and SQ4 true (−12 volts) enable the and gate consisting of diodes CR3 and $\overline{CR4}$ and pulldown resistor R2. The resulting true signal is coupled through resistor R3, which prevents clock pulse loading

of the logic inputs, and forward-biases clock pulse switching diode CR6 when the positive clock pulse appears. Diode CR6, when forward-biased, passes the clock pulse which is coupled through blocking capacitor C2 to the base of transistor Q2. This positive pulse reverse-biases the base-emitter junction of Q2 and causes it to cease conducting and allows its collector to rise to −12 volts. Transistor Q2 collector load R9, Q1 base current-limiting resistor R8, and resistor R6 form a voltage divider which allows a portion of the voltage change at the collector of Q2 to be coupled to the base of Q1. Speedup capacitor C4 allows the base capacitance of Q1 to be readily charged or discharged. Negative voltage at the base of Q1 forward-biases its base-emitter junction to allow collector current to flow. Increasing collector current causes the voltage at the collector of Q1 to drop to 0 volt. Transistor Q1 collector load R4, Q2 base current-limiting resistor R5, and R7 form a voltage divider which allows a portion of the voltage change at the collector of Q1 to be coupled to the base of Q2. This positive voltage further decreases Q2 collector current. This action continues until Q2 is entirely cut off and Q1 is saturated. At this time, SQ1 is false and $\overline{SQ}1$ is true. Signal $\overline{SQ}1$ true enables the or gate consisting of diodes CR1 and CR2. The resulting true signal causes Q1 to cease conducting and Q2 to conduct in the manner described above.

(2) *Flip-flops SQ2 and SQ3.* $\overline{SQ}1$ output of flip-flop SQ1 is applied to differentiator network C5, R14. When $\overline{SQ}1$ goes from the true (−12 volts) state to the false (0 volt) state, the differentiator network produces a positive pulse which forward-biases clock pulse gating diode CR8. The positive pulse is coupled through forward-biased CR8, through Q4 base current-limiting resistor R11, and speedup capacitor C6 to the base of Q4. The base-emitter junction of Q4 is reverse-biased by the positive pulse, and Q4 subsequently ceases conducting. The regenerative action which saturates Q3 and cuts off Q4 is the same as described for flip-flop SQ1. When $\overline{SQ}1$ again switches from the true to the false state, clock pulse gating diode CR9 is forward-biased by a positive pulse. This positive pulse causes Q3 to cease conducting and Q4 to conduct as described above. Flip-flop SQ3 operates in the same manner as SQ2.

b. Clamp Q7. When $\overline{SQ}4$ is true, 24 volts is applied across the voltage divider consisting of R22 and R23 which causes the base-emitter junction of Q7 to be forward-biased. The resulting current flow through Q7 places the anodes of diodes CR7, CR10, and CR11 at ground potential and causes them to conduct; this action places the SQ outputs of all three flip-flops at ground potential (false) and thus resets the counter.

c. $\overline{SP}2$ Gating. Signals SQ1, $\overline{SQ}2$, SQ3, and SQ4 true enable the and gate (consisting of CR14, CR15, CR16, CR17) and pulldown resistor R25. The resulting true signal is current-amplified by emitter follower Q8. The output of this circuit appears across Q8 emitter resistor R26.

d. IRP Gating. This circuit ands $\overline{SQ}4$ and $\overline{SQ}5$ and transforms the logic levels used on this assembly to standard logic levels. When $\overline{SQ}4$ and $\overline{SQ}5$ are both true (−12 volts), the output of the voltage divider formed by R27, R28, and R29 reverse-biases the base-emitter junction of Q9 and causes it to cease conducting. When current ceases to flow through collector load resistor R30, the collector voltage of Q9 rises toward +12 volts but is clamped to 0 volt by diode clamp CR18. When any of the inputs is at 0 volt, Q9 is forward biased and causes the output to go to −6 volts.

e. DCP Gating. The DCP gate consists of two circuits similar to the circuit described in *d* above, but with a common collector resistor. This gate ands $\overline{SQ}2$, $\overline{SQ}3$, SQ1, and SQ4 and transforms the logic levels to standard logic levels of −6 volts and 0 volt. Transistors Q10 and Q11 must both be in the nonconducting (cutoff) state before the output is true (0 volt).

65. Amplifier Demodulator, 1518428

(fig. 24)

a. General. The amplifier demodulator con-

verts 1,500-cps and 600-cps pulse code modulated signals to the dc logic levels required by the WMC and RDPC. The amplifier demodulator consists of input transformer T1, high-pass filter FL1, agc amplifier V1, amplifier V2, separation filter FL2, two full-wave rectifiers, and an automatic gain control (agc) circuit. The receiver message is coupled through impedance-matching input transformer T1, high-pass filter FL1 for noise rejection, and MESSAGE LEVEL adjust R10 to agc amplifier V1. The output of V1 is amplified by V2A and separated into 1,500-cps and 600-cps components by separation filter FL2. Each output of FL2 is full-wave rectified by diode bridges and smoothed into approximated square wave signals by FL3. The full-wave rectified 1,500-cps signal (data) is amplified by feedback amplifier V2B. The amplified feedback is clipped, half-wave rectified, filtered, and applied to the suppressor grid of V1 to control the gain of V1.

b. *AGC Amplifier Circuit.* The received message contains bursts or pulses of 600-cps and 1,500-cps signals. The primary of T1 has an input impedance of 600 ohms which matches the impedance of the ADL line. The secondary has an output impedance of 8,644 ohms which matches the input impedance of high-pass filter FL1. This impedance matching prevents ringing on the line and enables FL1 to remove low frequency noise. The output of T1 can be observed at TP1. The adjusted signal from R1 is applied through decoupling resistor R4 to the grid of V1. The amplified signal from V1 is supplied through coupling capacitor C2 to amplifier V2A. The control grid of agc amplifier V1 is biased at −4 volts by voltage divider R2, R3. The bias voltage is maintained at −4 volts by ac bypass filter capcitor C1. The gain of V1 is automatically controlled by application of a variable negative voltage to its suppressor grid. The magnitude of the negative voltage is a function of input signal strength. The screen grid bias is supplied from +150 volts through R6 to provide approximately +115 volts at the screen grid. Capacitor C3 maintains a constant screen grid voltage. Voltage divider R5, R19 provides +150 volts. Resistor R5 is the plate load resistor and R19 reduces the plate supply voltage when V1 is nonconducting during filament warmup for tube protection. The signal to the control grid of V1 can be observed at TP2.

c. *Amplifier and Demodulator Circuit.* The signal from V1 is applied to the control grid of V2A through coupling capacitor C2. The plate load for V2A is separation filter FL2, and the output of V2A can be observed at TP3. Cathode bias for V2A is provided by C4 and R8. Grid return resistor R7 provides a ground reference to the grid of V2A. Separation filter FL2 separates 600 cps from 1,500 cps in the signal and provides each as a center-tapped output. The 1,500-cps output is full-wave rectified by bridge CR1–CR4, and the 600-cps output is full-wave rectified by CR5–CR8. The output of the 1,500-cps bridge appears across R9 as pulse envelopes of 4 negative half cycles per time slot, and the 600-cps bridge output appears across R10 as 1 pulse of 5 negative half cycles per message. The output of each bridge is applied to low-pass filter FL3 which smooths the full-wave rectified signal into a pulse which generally resembles a square wave. The output of the 1,500-cps bridge is also supplied through coupling capacitor C5 to the input of feedback amplifier V2B.

d. *Feedback Amplifier Circuit.* The input to feedback amplifier V2B from C5 is basically a 3-kc sine wave (the 1,500-cps full-wave rectified signal produces a 3-kc ac signal). This feedback signal is amplified by V2B, rectified by CR10, filtered by C7, R16 and applied to the suppressor grid of V1. The AGC adjust (R12) provides the bias voltage to the control grid of V2B through grid decoupling resistor R11. The voltage available from R12 is variable from 0 volt to −28 volts which makes it possible to vary the conduction of V2B from relatively heavy conduction to cutoff. The amplified signal appears across plate load resistor R17 and is coupled through C6 to rectifier CR10 and clamping diode CR9. Resistor R13 provides a fixed bias of −4 volts to the cathode of CR10, and CR9 clamps the anode of CR10 to −4 volts during positive half cycles. When AGC-DISABLE switch S1 is in the AGC position, CR10 conducts during negative half cycles, charging C7. The discharge path of C7 is through R16 to the −4-volt bias line. The C7, R16 time constant is about 27 seconds so that suppressor grid voltage for V1 is relatively constant during any message. During agc operation, the minimum voltage on the suppressor grid is −4 volts from

the bias line. The maximum voltage on the suppressor grid, which is −11 volts, occurs with S1 in the DISABLE position. The suppressor grid voltage can be measured at TP5 and the input to V2B can be observed at TP4.

66. Slicer, 1518486

(fig. 27)

a. General. The ready and data slicer circuits (151846) shape the smoothed ready and smoothed data signals and also generate the complement of these signals. The ready and data slicer circuits are identical; therefore, only the data slicer is discussed. The ready slicer circuit equivalent elements are shown in the chart below. Each signal is shaped and its complement formed in a shaping (Schmitt trigger) circuit. A Schmitt trigger circuit has two stable states and is controlled by the amplitude of the input signal. The smoothed data signal from the amplifier demodulator is applied to amplifier Q1 in the slicer. Amplifier Q1 is a temperature-stabilized, variable-gain amplifier that controls shaper Q2, Q3 (Schmitt trigger). The amplitude of the signal from Q1 determines when Q2 is conducting or nonconducting. Transistor Q3 is always opposite in state of conduction from Q2. Slicer adjust R4 controls the gain of Q1 by changing its bias voltage. The gain of Q1 determines shaper triggering and, therefore, the output pulse width. Resistor R4 is adjusted so that the pulse width of the data output of the data slicer is one time slot wide (1.33 millisecond). The ready signal pulse width is not as critical. A negative smoothed data signal applied to Q1 causes Q2 to conduct and Q3 to be cut off. When the smoothed data signal is not present, Q2 is cut off and Q3 is conducting. The Q3 output is applied to emitter follower Q4, and the Q2 output is applied to emitter follower Q6. Transistor Q4 and Q6 current-amplify and clamp the outputs to 0 volt or −6 volts. The outputs of the emitter followers are routed to inverters Q5 and Q7. Inverters Q5 and Q7 invert and clamp the outputs to 0 or 12 volts. The outputs of the inverters are complements of each other and are the data and $\overline{\text{data}}$ signals.

Data slicer element	Ready slicer equivalent element
Q1–Q7	Q8–Q14
R1–R26	R27–R52
CR1–CR6	CR7–CR12
C1	C2
RT1	RT2

b. Temperature-Compensated Amplifier Circuit. The smoothed signal input to the slicer is either 0 volt or a negative pulse with rounded leading and trailing edges and either 1,200-cps or 3-kc ripple (frequency doubling results from full-wave rectification and filtering). Amplifier Q1 amplifies this signal to increase the volt-per-second rate of change in the leading and trailing edges and also inverts the signal: When the smoothed signal is 0 volt, Q1 is cut off; when the smoothed signal is sufficiently negative, Q1 conducts. With the input open, slicer adjust R4 may be adjusted to bias Q1 between −0.35 volt and +1.15 volt. With R4 adjusted for a −0.35-volt base bias, Q1 is near cutoff and changes conduction any time the smoothed signal changes negatively. With R4 adjusted for a +1.15-volt base bias, Q1 changes conduction when the smoothed signal becomes more negative than −1.7 volt. Adjustment of R4 thus controls the sensitivity of Q1 to noise as well as affecting its gain. Input resistor R1 is a current-limiting resistor which, with emitter resistor R6, increases the input impedance and reduces the sensitivity of Q1. Resistors R2, R3, R4, and thermistor RT1 form a temperature-compensating voltage divider which biases Q1 and limits the effect of temperature variations on Q1 operation. Thermistor RT1 has a large negative temperature coefficient so that its resistance decreases rapidly with increasing temperature and causes the base bias voltage to become more positive. This counteracts the tendency of Q1 to conduct more rapidly with increasing temperature. Resistor R5 is the collector load resistor, connected for negative feedback through R2 to the base of Q1. The smoothed signal input can be observed at TPB–1.

c. Shaper Circuit. Shaper circuit Q2, Q3 is a Schmitt trigger the output states of which depend on the amplitude of the input signal. The base if

Q3 is biased at approximately −21.8 volts by voltage divider R7, R10, and R11. Resistors R9, R12 and capacitor C1 help to keep the junction of R8 and R11 at approximately −27 volts. With Q3 forward biased, the emitters of both transistors are at 21.6 volts due to the emitter-base voltage drop of Q3. If the input voltage at the base of Q2 is less than approximately 21.8 volts, Q2 is off. When the input voltage level goes above 21.8 volts, a critical level is reached and Q2 begins to conduct. With Q2 now drawing current, the voltage at the emitters goes more positive and the voltage at the collector of Q2 goes more negative. This condition quickly turns off Q3. When the input voltage now goes below another critical value, Q3 will again conduct and Q2 will cut off. Switching action in Schmitt trigger Q2, Q3 is rapid because of the large regenerative feedback and the outputs of Q2 and Q3 are complementary square wave signals. The collector voltage of Q2 is supplied to emitter follower Q6 and the collector voltage of Q3 is supplied to Q4.

d. Emitter Follower Circuits. The two emitter follower circuits are identical, so only the Q4 circuit is discussed. The shaped signal from Q3 is supplied through current-limiting resistor R15 to the base of Q4. The base of Q4 is positively clamped by CR1 and R16 to approximately ground potential. The output of Q4 is negatively clamped to −6 volts by CR2. Emitter resistor R17 is a current limiter. When the Q3 output signal is negative, CR1 is cut off and Q4 conducts; however, current flow through R17 is not enough to pull the emitter of Q4 above −6 volts and the Q4 output is therefore clamped to −6 volts by CR2. When the Q3 output goes to 0 volt, CR1 is forward biased and clamps the base of Q4 to ground. Transistor Q4 conducts heavily and places its emitter at close to 0 volt and cuts off CR2. The sliced signal from Q4 can be observed at TPB–2 and the sliced signal from Q6 can be observed at TPB–3. The output signals from Q4 and Q6 are routed to inverters Q5 and Q7.

e. Inverter Circuits. The two inverter circuits are identical; so only the Q5 circuit is discussed. The sliced signal from Q4 is supplied through input resistor R18 to the base of Q5. Resistor R19 provides bias for Q5. When the input to Q5 is −6 volts, Q5 conducts heavily and its collector is clamped to approximately ground potential. When the input to Q5 is 0 volt, Q5 is cut off and the collector of Q5 is clamped to −12 volts by CR3.

67. Detector Start/Remote, 1522348

(fig. 32)

a. General. The start/remote detector comprises three circuit groups: ready start detector, remote start detector, and control. The ready start detector circuit consists of logic converter Q9, integrator Q10, ready start switch Q11, negative and gate Q4, and inverter Q5 (not used). The remote start detector circuit consists of logic converter Q16, integrator Q17, remote start switch Q18, negative and gate Q13, and switch Q14 (not used). The control circuits that are common to both of the circuit groups mentioned above are integrator resets Q15, MFC one-shot multivibrator Q1, Q2, inverter Q3, emitter follower Q6, and switches Q7 and Q8. The inputs to the start/remote detector are MFC, $\overline{\text{MFC}}$, and ±3-volt detector (det) signals from 1,500-cps detector 1518325 (para. 61), and reset signals (para. 27). The ready start circuit detects the −3-volt detector signal to generate the $\overline{\text{ready start}}$ output, and the remote start circuit detects the +3-volt detector signal to generate the remote start output. The MFC, $\overline{\text{MFC}}$, and reset signals are used by the control circuits to gate or reset either the $\overline{\text{ready start}}$ output signal or the $\overline{\text{remote start}}$ output signal.

b. MFC One-Shot Multivibrator Q1, Q2. The MFC one-shot multivibrator receives the MFC signal from the 1,500-cps detector. The MFC signal is differentiated by input capacitor C1 and resistor R1. The negative, trailing edge of the differentiated MFC signal forward-biases diode CR1 and is applied to the base of transistor Q1. A negative voltage at the base of Q1 forward-biases Q1 and causes current flow through collector load R3. The voltage drop across R3 causes the collector voltage to go positive (approximately 0 volt). Transistor Q2 is normally conducting and the voltage drop across base bias resistor R4 causes the base voltage of Q2 to be slightly negative. A positive-going voltage at the collector of Q1 is coupled through capacitor C2 to the base of Q2. A positive potential at the base of Q2 cuts Q2 off and prevents current flow through collector load resistor R5. With no voltage drop across R5, the collector of Q2 goes negative. The negative

voltage is applied through input resistor R7 to the base of inverter Q3 and also through feedback resistor R6 to the base of Q1. The negative feedback voltage aids the incoming negative pulse admitted through CR1 and holds the collector of Q1 near 0 volt. Before the MFC pulse enters the one-shot multivibrator, capacitor C2 is charged up to 12 volts; the Q1 (left) side is negative with respect to the Q2 (right) side. At the trailing edge of the MFC pulse, the collector of Q1 goes to 0 volt and C2 begins to discharge through Q1 and R4. The instant the collector of Q1 goes to ground potential, 24 volts is impressed across R4, which places the base of Q2 at +12 volts and immediately cuts it off. Transistor Q2 remains nonconducting and its collector goes negative and remains that way until the potential at the base of Q2 goes slightly negative. The time needed for C2 to discharge completely and begin charging in the opposite direction (so that the base of Q2 can go negative) is approximately 5 milliseconds. After this time has elapsed, Q2 begins to conduct and causes its collector to go to 0 volt, which cuts off Q3 and Q1. The circuit remains in this state until the next MFC pulse comes along.

c. Inverter Q3. When the collector voltage of Q2 initially goes negative, negative voltage is applied through input resistor R7 to the base of transistor Q3. The voltage developed across resistor R3 establishes the base bias of Q3. A negative voltage at the base of Q3 forward biases Q3 and causes current flow through collector load R9. The voltage drop across R9 causes the collector voltage of Q3 to become 0 volt. When the collector voltage of Q2 goes in a positive direction, this voltage is applied to the base of Q3 through R7 to reverse-bias Q3 and prevent current flow in its collector circuit. With no current flow through Q3, its collector goes to −7 volts. The output, taken at the collector of Q3 (TP1), is a positive-going pulse (−7 volts to 0 volt) of 5 millisecond duration and is routed to negative and gate Q4.

d. Ready Start. Logic converter Q9 receives and converts −3-volt detector signals from the 1,500-cps detector into voltage levels for use by integrator Q10. The output of Q10 controls the action of ready start switch Q11.

(1) When ready frequency (ready start) is received by the demodulator, 0 volt is applied to the voltage-divider network composed of input resistor R26 and base bias resistor R27, which applies a positive voltage to the base of Q9 and causes Q9 to conduct. The voltage-divider action of R29 and R28 causes the base of Q10 to decrease toward +6 volts from its previous level of +12 volts. The emitter of Q10 is held at slightly less than +12 volts by constant voltage source R31, CR7. When the base of Q10 reaches approximately +11 volts, Q10 begins conducting. Current flows through collector load resistor R30 and causes the Q10 collector to go toward the +11.5-volt potential at its emitter. The voltage at the collector of Q10 is applied through input resistor R32 to the base of ready start switch Q11 (TP4).

(2) When a mark frequency is received by the demodulator, −7 volts is applied to the voltage-divider network, consisting of R26 and R27. The voltage-dividing action of R26 and R27 places approximately −4 volts on the base of Q9, and Q9 is cut off. With Q9 at cutoff, +12 volts appears on the base of Q10, and Q10 cuts off. With Q10 at cutoff, a negative voltage is applied to the base of Q11 through input resistor R32.

e. Ready Start Switch Q11. Ready start switch Q11 controls the gating of the inverter Q3 output through negative and gate Q4.

(1) Just before a ready start signal is received by the demodulator, Q9 is cut off, integrator Q10 is cut off, and a negative voltage applied to the base of ready start switch Q11 keeps it conducting. At this time, there is no reset pulse from Q15, and the top capacitor C3 is at a small negative voltage because of the small voltage drop across base-emitter junction of Q11. Capacitor C3 is therefore charged to 12 volts; its top is negative with respect to its bottom as seen on figure 32. Current flows through collector load resistor R33 and causes its collector output voltage to be at 0 volt. The Q11 collector output is sent to negative and gate Q4 where it is gated with the output of inverter Q3. At this time,

the R3 output is −7 volts and the negative and gate output is 0 volt.

(2) When the −3-volt detector logic signal goes positive (ready or space signal received), Q9 conducts and causes Q10 to conduct and its collector to rise to +12 volts. Capacitor C3 starts to discharge through R32, Q10, and CR7 and the potential at the base of Q11 rises toward +12 volts. As soon as C3 begins to discharge, the voltage at the base of Q11 is not negative enough to keep Q11 conducting and it cuts off. To insure that C3 is fully discharged, so that circuit timing is kept to predetermined values, a +12-volt reset pulse from Q15 forward-biases diode CR12 and causes C3 to quickly discharge and place +12 volts on the base of Q11. The Q11 collector voltage (−12 volts) is sent to negative and gate Q4 to be gated with the Q3 output. At this time, the Q3 output is still −7 volts and the negative and gate output is 0 volt.

(3) When the −3-volt detector logic signal goes negative again (end of ready start), Q10 is again cut off and C3 starts to charge. When the voltage at the base of Q11 (top of C3) reaches a slightly negative potential, Q11 begins to conduct. The collector of Q11 goes to 0 volt, and this potential is applied to negative and gate Q4.

f. Negative and Gate Q4 and Inverter Q5. The 0-volt outputs from Q3 and Q11, through input resistors R10 and R12, respectively, cause Q4 to cut off, which produces a −12-volt output. If the inputs to Q4 are opposite states or are both −12 volts, Q4 saturates and its output is 0 volt. Resistor R13 is the collector load resistor for Q4; R11 and the +12-volt supply provides cutoff bias for Q4. Inverter Q5 inverts the output of negative and gate Q4. When the negative and gate output is 0 volt, 0 volt is applied to the base of Q5 through input resistor R14. Resistor R15 and the +12-volt supply provides base bias for Q5. With 0 volt on its base, Q5 is cut off, and no collector current flows in the collector circuit. Diode CR2 becomes forward-biased and conducts. Current flows from the −28-volt supply through collector load resistor R16, voltage-divider resistor R17, and diode CR2 to the −12-volt supply. When the negative and gate output is −12 volts, −12 volts is applied to the base of Q5 through input resistor R14. With −12 volts on its base, Q5 is forward-biased, and current flows from the −28-volt supply through R16. The 0-volt collector voltage causes CR2 to be back-biased; therefore, the output of Q5 is 0 volt.

g. Integrator Reset Switch Q15. Integrator reset switch Q15 receives the $\overline{\text{MFC}}$ signal from assembly 559955 (1,500-cps detector). When the MFC signal goes positive from 2 to 2.5 milliseconds after the start of the sync word, the $\overline{\text{MFC}}$ signal goes negative (−10 volts). At the instant the input voltage changes from 0 volt to −10 volts, the change is felt across bias resistor R46 and applied to the base of Q15. The emitter of Q15 is kept at a +12-volt level by constant voltage source R53, CR14. The leading edge of the $\overline{\text{MFC}}$ signal, therefore, causes Q15 to conduct and +15 volts is put on its collector. Up to this time, C3 was still in the process of discharging through the long-time constant path of R32, Q10, and CR7. When Q15 conducts, CR12 is forward-biased and C3 immediately discharges completely to bring the base of Q11 up to 12 volts in preparation for the entrance of the mark portion of the sync word. As soon as C4 charges completely, Q15 is again cut off.

h. MFC Clamp Circuit. The MFC clamp circuit (Q6–Q8) clamps the output of MFC one-shot multivibrator to 0 volt when the reset signal (para. 27) at pin $\overline{\text{E}}$, $\overline{\text{D}}$, or $\overline{\text{F}}$, goes to 0 volt. The input circuit to emitter follower Q6 is an or gate comprising CR4, CR5, CR6, and resistor R19. The reset signals are fed through CR4, CR5, and CR6 respectively to emitter follower Q6. If any of the reset signals go true (0 volt), the output of Q6 is 0 volt. The Q6 output is −6 volts only when all reset signals are false (−6 volts). When the Q6 output is at −6 volts, switch Q7 saturates and switch Q8 is cut off; the reverse is true when the Q6 output is at 0 volt. Resistors R20 and R23 are the load resistors for Q6 and Q7 respectively. The base current-limiting resistors for Q7 and Q8 are R21 and R24 respectively. Resistor R22 (at the base of Q7) and resistor R25 (at the base of Q8) are connected to +12 volts to provide cutoff bias.

i. Remote Start. The circuits used to detect a remote start in an incoming message are similar to the circuits that detect the ready start signal de-

scribed in *d*, *e*, and *f* above. A chart listing the corresponding components between the two circuits is shown below; similar circuit analysis described in *d*, *e*, and *f* above is applicable for the circuits used to detect remote starts.

Ready start detection	Remote start detection
Q9	Q16
R26	R48
R27	R49
Q10	Q17
R28	R51
R29	R50
R30	R52
R31	R53
CR7	CR14
Q11	Q18
R32	R54
C3	C5
CR12	CR13
R33	R55
Q4	Q13
R10	R36
R12	R37
R11	R38
R13	R39

Section III. POWER SUPPLY SUBFUNCTION

68. Plus and Minus 12-Volt Power Supply, 1512530

(fig. 20)

The ±12-volt power supply consists of an unregulated power supply that supplies both plus and minus unregulated 12 volts and a +12-volt regulator that contains a voltage-control multivibrator circuit, a switch circuit, a filter circuit, and an overload protection circuit. The regulating element used here is a transistor operating as a series switch. Variable duty cycle switching is employed to provide the necessary dc voltage regulation.

a. Unregulated Power Supply. System power of 120 volts ac, 400 cps is applied to the primary (pins 1 and 2) of power transformer T1. A voltage of about 19 volts ac, developed across each of the secondary windings N2 (pins 3 and 4) and N3 (pins 5 and 6) of T1, is applied to two bridge rectifier circuits that consist of CR13 through CR16 and CR17 through CR20. Filter capacitor C13 in parallel with the output of the first bridge rectifier, and filter capacitor C14 in parallel with the output of the second bridge rectifier, reduce ripple in their respective unregulated output voltages. The output at both filter capacitors is an unregulated dc voltage of 24-volt magnitude. Fuses F1 and F2 prevent damage, to either the power transformer or the bridge rectifier diodes, resulting from excessive loading of the output. The output of bridge rectifier CR13–CR16 is used in this assembly to provide +12-volt regulated power. The output of bridge rectifier CR17–CR20 is used by this assembly in conjunction with −12-volt regulator and protection circuit 1512552, J6A to provide −12-volt regulated power.

b. Voltage-Control Multivibrator Circuit. The voltage-control multivibrator circuit controls the output voltage by controlling the time that +12-volt switch Q13 is on. Differential amplifier Q4, Q8 compares the output voltage level with a voltage reference and controls the switching times of multivibrator Q5, Q7. Any change in the output voltage level is sensed by the differential amplifier. The differential amplifier generates a correction voltage to change the on-off times of multivibrator transistors Q5, Q7. The change in on-off times brings the output voltage level back to the desired level. Zener diode CR2, used in conjunction with C2, R9, and R10, provides a voltage of 9.1 volts for use by the multivibrator, differential amplifier, and overload protection circuits. Diode CR3, together with C3 and R11, produces 6.2 volts. The 6.2 volts is used as a constant voltage reference for the differential amplifier. Voltage adjust R12 sets the reference voltage applied to the base of Q4 of the differential amplifier. The differential amplifier compares the voltage at the base of Q4 with the voltage at the base of Q8. The voltage at Q8 which is nearly identical to the base voltage of Q4 is +3.75 volts because of voltage divider resistors R16 and R17 placed across the output of the +12-volt regulator. The voltages at the bases of Q4 and Q8 determine the amount of

conduction of the transistors. Constant current source Q6 acts as an infinite resistance with respect to an external circuit connected to its terminals. When the forward bias on either Q4 or Q8 increases, increased current is caused to flow in the transistor whose bias has increased. This action causes the voltage drop across Q6 to increase. The increased voltage drop across Q6 causes the forward bias on the transistor whose bias has not increased, to decrease. *For example*, if the voltage at the base of Q8 goes less positive because of a decrease in the output voltage, the current through Q8 will increase. The increase in current causes an increase in the voltage drop across Q6 and causes the emitter of Q4 to go less positive. The decrease in forward bias on Q4 decreases the amount of current. The base of Q6 is supplied with approximately +4 volts, as a result of R14, R18, and Q9. This condition puts the Q6 emitter at approximately 4.25 volts and the Q6 collector at approximately +4 volts. The collectors of Q4 and Q8 are connected to the base of multivibrator transistors Q5, Q7. The multivibrator acts as an output load for the differential amplifier and the differential amplifier transistors serve as base return resistances for Q5 and Q7. The multivibrator switches on and off at a nominal frequency of 45 kc. The on-off times of Q5 and Q7, however, are not necessarily equal and depend on the difference signal supplied by the differential amplifier. Consider Q5 *on* and Q7 *off*. With Q5 saturated, its collector is at 0 volt. With Q7 not conducting, its collector is at +9 volts. Capacitor C4 has charged up to 9 volts through R15 and the base-emitter junction of Q5. Capacitor C6 is discharging through Q8 of the differential amplifier. When C6 has discharged to a point where the potential at the base of Q7 goes slightly positive with respect to the emitter, Q7 starts to conduct and the collector of Q7 goes to 0. Capacitor C4, having been charged up to 9 volts, now discharges through Q4 of the differential amplifier which cuts off Q5. Transistor Q5 remains off and Q7 remains on until C4 has discharged to a point where the base of Q5 is slightly positive with respect to the emitter, when switching again takes place. The time the multivibrator transistors remain in their respective states depends on the discharge paths of C4 and C6. The discharge path of C4 is controlled by Q4. The discharge path of C6 is controlled by Q8. If the forward bias on Q8 increases, Q8 will act as a smaller resistance and allow C6 to discharge faster and Q7 to turn on faster. If the forward bias on Q8 decreases, C6 takes longer to discharge and Q7 remains off for a longer period of time. Capacitor C4, Q5, and C4 act in the same manner. Multivibrator turn-on Q9 eliminates the possibility of both Q5 and Q7 saturating when power is initially turned on. When Q5 and Q7 are both saturated, CR8 and CR9 are both reverse-biased with 0 on their anode and some positive voltage on their cathode. This condition causes Q9 to cease conducting. When Q9 ceases to conduct, supply voltage for the constant current source is interrupted and causes base current in both Q5 and Q7 to cease flowing. When the collector voltage of either Q5 or Q7 rises sufficiently to forward bias CR8, Q9 is turned on and the voltage-controlled multivibrator operates normally. Capacitor C5 is used to reduce ripple at the input to constant current source Q6.

c. Switch Circuit. The +9-volt input from the voltage-controlled multivibrator is coupled through base current-limiting resistor R22 and speedup capacitor C8 to the base of Q11. When this signal is positive, Q11 conducts and causes sufficient current to flow through its collector resistors (R21 and R27) to cause the switch drive signal to be about +15 volts. When the +9-volt square wave signal is at 0 volt, Q11 is cut off to cause the switch drive signal to be about +24 volts. Negative-going transitions on the +9-volt square wave signal are coupled through blocking capacitor C7 and base current-limiting resistor R24 to the base of Q10. Negative-going voltage at the base of Q10 causes it to conduct to divert current from Q11 away from resistor R21 and allow the base of Q13 to go positive more quickly. Transistor Q10 conduction also removes stored charge from the base of switch Q13 to allow it to cut off that much quicker. When a positive transition occurs on the +9-volt square wave input, Q10 is cut off. Diode CR7 conducts to allow C7 to adjust to the new voltage level across it, without damaging the transistor. Resistor R29 is in the circuit to allow a negative-going transition to be felt across it and thus provide Q10 with a forward bias. The overload signal input to this circuit from the overload protection circuit clamps the base of Q11 to ground potential and prevents it from conducting. Diode CR10 provides temperature stability for

switch driver Q11. Diodes CR5 and CR6 and resistor R23 form a voltage-divider network which reverse-biases the base-emitter junction of +12-volt switch Q13, when the switch drive input to this circuit is at about +24 volts. When the switch drive input is at about +15 volts, the base-emitter junction of Q13 is forward-biased and causes Q13 to conduct.

d. Filter Circuit. When Q13 conducts, CR11 is reverse-biased. The collector current of Q13 flows through choke L1 and charges filter capacitors C9 and C10. When Q13 ceases to conduct, the electromagnetic field around L1 collapses. This collapsing field generates a voltage which forward-biases CR11 and continues to charge C9 and C10. When a malfunction occurs which causes the +12-volt regulated output of this circuit to rise to 15 volts or greater, CR21 conducts heavily and causes an overload condition, which disables the supply. Bleeder resistor R30 provides a constant minimum current flow by providing a discharge path for C9 and C10.

e. Overload Protection Circuit. Under normal operation (no overload), the voltage divider, consisting of R1 and R2, forward-biases the base-emitter junction of transistor Q1. At this time, the voltage developed across sensing resistor R9 is less than 1.8 volt. The collector voltage of Q1, now saturated, is about 0 volt with respect to the common 12-volt return. With Q3 drive current flowing through R6 and R7, TP1 or the cathode of CR4 is at about +12 volts. The anode of CR4 is at either 0 volt when Q5 is conducting or +9 volts, when Q5 is cut off. In either case, the cathode of CR4 is positive with respect to its anode and it does not conduct. It therefore has no effect on switch driver Q11 and regulation takes place in its usual way. When an overload occurs, excessive current passing through R9 develops a voltage which causes Q1 to be cut off. The collector of Q1 rises toward a positive voltage and causes C1 to charge through R4. When C1 is sufficiently charged, the base-emitter junction of Q2 becomes forward-biased and causes Q2 to conduct. The collector of Q2 drops to about 0 volt, which forward-biases diode CR4 and provides the overload protection circuit output signal to the switch driver circuit. The output signal holds the base of switch driver Q11 at near 0 volt, which causes Q11 and +12-volt switch Q12 to be held in a nonconducting state. Zero volt at the junction of R6 and R7 cuts off Q3 and causes its collector to rise toward +24 volts. The positive voltage on the collector of Q3 forward-biases diode CR1 and provides a positive base voltage, which together with the positive base voltage supplied by R3, R4, and R5, holds Q2 in saturation. When the overload is removed, Q1 again conducts, and C1 discharges somewhat through Q1 and R4. Transistor Q2 remains in saturation and Q3 remains at cutoff, due to the positive feedback provided by diode CR1. When S1 is pressed (after the overload has been removed), Q3 saturates, which reverse-biases CR1 and allows Q2 to return to its normally nonconducting state.

f. Minus 12-Volt Regulator Circuitry. The remaining circuitry on 1512530 is part of the −12-volt regulator and protection circuit (para. 69). Its operation is similar to the operation of the circuitry used for the +12-volt regulator.

69. Minus 12-Volt Regulator and Protection Circuit 1512530 and 1512552

(figs. 20 and 21)

The −12-volt power supply operates as described for the +12-volt regulated power supply (para. 68); however, the physical location of the components and, in some cases, the reference designators for the components, are different. The unregulated power supply, the −12-volt switch, and filter circuit are located on assembly 1512530 (fig. 20). The remainder of the components are located on assembly 1512552. The following chart of similar components lists only those components having different reference designators. Identical components (those with the same reference designators) are not listed.

+12-volt supply	−12-volt supply
T1(3–4)	T1(5–6)
CR13	CR17
CR14	CR18
CR15	CR19
CR16	CR20
F1	F2
C13	C14
Q13	Q14
CR11	CR12
C9	C11
C10	C12
CR21	CR22
R30	R31
L1	L2

CHAPTER 7

TROUBLESHOOTING

Section I. GENERAL TROUBLESHOOTING INFORMATION

70. Introduction

a. The information in this chapter is to enable maintenance personnel to locate and repair malfunctions in a transmitter-receiver. The troubleshooting procedure used in this manual is based on the assumption that all of the input and output buffers of the RDPC and WMC are operating correctly. Before using this procedure, insure that the trouble is in the transmitter-receiver by using the subsystem maintenance information (TM 11-5840-271-30/18 or TM 11-5840-272-30/17).

b. Once a trouble is found to be in a specific transmitter-receiver, figures 1 through 4 can be used to give maintenance personnel a general description of how the malfunctioning unit ties in with other RDPC or WMC functions which feed it or receive its output signals. After isolating the malfunctioning transmitter or receiver, perform the general troubleshooting procedures outlined in paragraph 75 before going to the respective troubleshooting section for the receiver or transmitter.

71. Reference Data

The following data will be helpful to the repairman when troubleshooting the transmitter and receiver:

a. Detailed Functional Block Diagrams (figs. 37-41). The detailed functional block diagrams give the electrical interrelationships among the components and stages for the transmitter-receiver. They also contain test points which can be used in testing for signals which travel in and between cards. By the observation of symptoms and the reasoning of possible causes, the cause of faulty operation can generally be isolated to a card assembly. Whenever possible, use the detailed functional block diagrams in conjunction with the troubleshooting charts.

b. Subsystem Maintenance Information. Refer to the subsystem maintenance information volumes (TM 11-5840-271-30/18 for the RDPC and TM 11-5840-272-30/17 for the WMC) for general maintenance information. Do not attempt to troubleshoot the transmitter and receiver without a thorough knowledge of the data contained in the subsystem maintenance information volumes.

c. Vacuum Tube Voltage and Resistance Diagram (fig. 35). The vacuum tube voltage and resistance diagram gives normal voltage and resistance measurements at all tube socket pins and is an aid in determining conditions and in evaluating clues in the course of troubleshooting. When using the diagram, carefully read the notes and exactly duplicate the conditions under which the readings were obtained.

d. Amplifier Demodulator Chassis Parts Location Illustration (fig. 36). This illustration is helpful when components are replaced in amplifier demodulator chassis 1518428, because it shows the exact location of the component.

e. Dc Resistance of Transformers and Coils. Refer to TM 11-5840-271-30/18 (RDPC) or TM 11-5840-272-30/17 (WMC) for charts showing the dc resistance of transformers and coils in the transmitter-receiver.

f. Color Code Diagrams. Refer to TM 11-5840-271-30/18 (RDPC) or TM 11-5840-272-30/17 (WMC) for color coding chart of plug-in circuit cards and resistors or capacitors.

g. Waveforms. Figures 33 (FSM) and 34 (PCM) provide voltage waveforms which should be observed at certain test points within the 502602.

h. Card Assembly Schematic Diagrams. The following chart lists the card assemblies in the

transmitter-receiver and the figure number of the card assembly schematic diagrams.

Card assembly	Figure No.
1512530	20
1512552	21
1518302	22
1518303	23
1518324	15
1518325	18
1518326	16
1518327	17
1518428	24
1518471	25
1518484	26
1518486	27
1518493	28
1518494	29
1522307	29
1522312	31
1522348	32
547885	13
549591	14
593982	19

72. Tools Required

Tool Kit TK–105/MSQ–28, supplied with Electronic Shop, Semitrailer Mounted AN/MSM–34 and available to the RDPC and WMC, is required for field maintenance of the transmitter-receiver.

73. Test Equipment Required

The chart below lists the items of test equipment that are required to maintain the transmitter-receiver. The chart also lists the literature that covers each item and gives a brief description of the use of each item.

74. Preliminary Checks and Control Settings

When troubleshooting the RDPC transmitter-receiver, set all RDPC controls to the positions indicated in the preliminary checks and control settings portion of the RDPC subsystem maintenance information manual (TM 11–5840–271–30/18). When troubleshooting any of the three WMC transmitter-receivers, set all WMC controls to the positions indicated in the preliminary checks and control settings portion of WMC subsystem maintenance information manual (TM 11–5840–272–30/17).

75. General Troubleshooting Procedure

The troubleshooting procedures in this chapter are based on the assumption that all supply voltages and message input signals are present. The following charts provide checkpoints where the voltages and message inputs may be checked. Before attempting to use the troubleshooting procedures (paras. 76 through 81), check these voltages and message inputs.

a. Voltage Input Chart. The following chart lists all voltage inputs to transmitter-receiver 502602. If any voltage is abnormal, see TM 11–5840–273–30.

Test equipment	Technical manual	Use
Oscilloscope AN/USM–81	TM 11–6625–219–12	Waveform observations.
Multimeter AN/URM–105	TM 11–6625–203–12	Voltage measurements.
Test Set, Electronic Circuit Plug-in Unit TS–1712/MSQ–28.	TM 11–6625–430–12	Standard plug-in card assembly tests.

Voltage	Checkpoint
+1.5	TP33B
+28	TP32B
+50	TP31B
+150	TP30B
+300	TP29B
−6	TP35B
−7.5	TP36B
−26.5	P1–20
−28	TP37B
−50	TP38B
120 vac, 400 cps	P1–30
Ac return	P1–21

b. Regulated Voltages. The transmitter-receiver contains three Zener diode voltage regulators as part of its power supply subfunction: +27 volts, −27 volts, and +18 volts. The following chart lists the checkpoints and card assemblies to be checked if the regulated voltages are abnormal. The voltages checked in *a* above are used to generate the regulated voltages; therefore, these voltages must be checked prior to checking the regulated voltages.

c. Power Supply, ±12 Volts. Each transmitter-receiver contains a +12-volt power supply and regulator and a −12-volt power supply and regulator. The regulated ±12 volts is used throughout the transmitter-receiver and must be available for proper operation. The ±12-volt power supplies depend on 120 volts ac, 400 cps.

Voltage	Checkpoint	Remarks
+18v regulated.	TP34A	If abnormal, check 1518484, J10A–J11A.
+27v regulated.	TP32A	If abnormal, check 549591, J14A–J17A.
−27v regulated.	TP33A	If abnormal, check 1518484, J10A–J11A.

Voltage	Checkpoint	Remarks
+12v regulated.	TP29A	If abnormal, check 1512530, J1A–J5A.
−12v regulated.	T30A	If abnormal, check 1512530, J1A–J5A, and 1512552, J6A.

d. Receivers A and B Message. The transmitter-receiver receives modulated messages (either PCM or FSM) from an associated communications central cabinet or input buffer (para. 70) and demodulates and synchronizes the message. The chart below shows the checkpoints where the incoming messages can be monitored to verify that the transmitter-receiver is receiving the proper message. If the message input is abnormal, the trouble is probably located in the associated communications central cabinet or input buffer.

Checkpoint	Normal indication
Insert oscilloscope channel A probe into TP21B for receiver A (TP21C for receiver B). Place oscilloscope ground probe into TP22B for receiver A (TP22C for receiver B). Sync oscilloscope text at TP21B for receiver A (TP21C for receiver B).	*a. PCM Messages.* Complete message is 82 time slots long. Sync word (TS0–TS7) consists of three time slots of 1,500 cps mixed with 600 cps followed by three time slots of 1,500 cps, one blank time slot, and then one time slot of 1,500 cps. The remainder of the message consists of one time slot of 1,500 cps for each true data bit. *b. FSM Messages.* Complete message is 83 time slots long. Sync word (TS00–TS7) consists of four time slots of 1,500 cps followed by three time slots of 1,125 cps, one time slot of 1,875 cps, and then one time slot of 1,125 cps. The remainder of the message consists of one time slot of 1,125 cps for a mark and one time slot of 1,875 cps for a space.

e. Transmitter Message. The transmitter-receiver receives digital messages (data control and ready control signals) from the communications central or associated output buffer (para. 70), modulates the digital message (either in PCM or FSM), and routes the modulated message to the associated communications central. The data control signal is checked at TP15A and the ready control signal is checked at TP17A. The data control signal is a train of true and false signals with 0 volt being a true and −15 volts being a false data bit. The ready control signal is at 0 volt for four time slots in FSM mode and three time slots in PCM mode. After the three (PCM) or four (FSM) time slots, the ready control signal goes to −15 volts for the remainder of the message. When there are no messages to be transmitted, the data control signal is at 0 volt and the ready control signal remains at −15 volts.

Section II. RECEIVER SUBFUNCTION TROUBLESHOOTING

76. General

The receiver subfunction receives a modulated message, demodulates the message, and synchronizes the demodulated message to an internally generated 6-kc clock pulse. Three main signals are supplied by the receiver subfunction: synchronized data, input ready pulse, and delayed clock pulse. A trouble in the receiver subfunction causes one or all of these signal outputs to be abnormal. The receiver subfunction isolation chart (para. 77) checks all of the signal inputs necessary to generate the synchronized data, input ready pulse, and delayed clock pulses. When a trouble is suspected in the receiver subfunction, make the signal checks outlined in the isolation chart. If all signals checked in the isolation chart are normal, the problem is in the synchronizer circuits; troubleshooting steps 9 through 12 in paragraph 78 isolate the trouble. If any of the signals checked by use of the isolation chart are abnormal, the *Remarks* column shows the troubleshooting step to proceed to in paragraph 78.

77. Receiver Subfunction Isolation Chart

Note: RECEIVER FSM–PCM/SELECT switch on 1522307, J20B for receiver A, and J19C for receiver B, set to PCM.

Signal checked	Checkpoint	Oscilloscope sync point	Normal indication	Remarks
Data PCM rcvr	Rcvr–A TP3B, rcvr–B TP3C.	+Ext rcvr A TP21B rcvr B TP21C.	Signal is at Ov for ≈8 milliseconds then goes to −12v for 1.33 milliseconds, and to Ov for 1.33 milliseconds. The remainder of the message consists of 1.33 milliseconds at 0 volt for each true data bit and 1.33 milliseconds at −12v for each false data bit.	If abnormal, see step 5, para. 78.
$\overline{\text{Data}}$ PCM rcvr	Rcvr–A TP4B, rcvr–B TP4C.	Same as data	Signal is logical complement of data signal.	If abnormal, see step 6, para. 78.
Ready PCM rcvr	Rcvr–A TP5B, rcvr–B TP5C.	+Ext rcvr A, TP23B, rcvr B TP22C.	Signal is at Ov for approximately 4 milliseconds and then goes to −12v for remainder of message.	If abnormal, see step 7, para. 78.
$\overline{\text{Ready}}$ PCM rcvr	Rcvr–A TP6B, rcvr–B TP6C.	Same as ready	Signal is logical complement of ready signal.	If abnormal, see step 8, para. 78.
Data FSM rcvr	Rcvr–A TP16B, rcvr–B TP16C.	+Ext rcvr A TP21B, rcvr B TP21C.	Signal is at Ov for ≈9.33 milliseconds and then goes to −12v for 1.33 milliseconds and to Ov for 1.33 milliseconds. The remainder of the message is Ov for each true bit in the message.	If abnormal, see step 1, para. 78.
$\overline{\text{Data}}$ FSM rcvr	Rcvr–A TP17B, rcvr–B TP17C.	Same as data	Signal is logical complement of data signal.	If abnormal, see step 1, para. 78.
Ready $\overline{\text{start}}$ rcvr	Rcvr–A TP20B, rcvr–B TP20C.	+Ext rcvr A TP22B, rcvr B TP22C.	Signal is at Ov for approximately 9.3 milliseconds and then goes to −12v for a maximum of 166 μsec and then returns to Ov for remainder of message.	If abnormal, see step 4, para. 78.
Remote start rcvr	Rcvr–A TP15B, rcvr–B TP15C.	Same as ready	Negative 166-μsec pulse	If abnormal, see step 4, para. 78.

78. Receiver Subfunction Troubleshooting Chart

Step	Symptom	Checkpoint	Sync oscilloscope	Normal indication	Procedure if abnormal indication observed
1	Data, or $\overline{\text{data}}$, abnormal.				
	a. Receiver A	*a.* Channel A TP21B, channel B TP1 on 1518325, J17B–J18B.	*a.* +Ext TP21B.	*a.* Refer to FSM receiver timing diagram (fig. 8). Note that the BBD signal is delayed from the input message at TP21B by from 3 to 5 milliseconds.	*a.* If BBD signal is normal, check 1518327, J15B–J16B. If BBD signal is abnormal, perform steps 2 and 5.
	b. Receiver B	*b.* Channel A TP21C, channel B TP1 on 1518325, J16C–J17C.	*b.* +Ext TP21C.	*b.* Same as step *a* above	*b.* Same as step *a* above except assembly 1518327 for receiver B is located in J14C–J15C.
2	BBD signal abnormal.				
	a. Receiver A	*a.* Channel A TP21B, channel B TP3 on 1518326, J13B–J14B.	*a.* +Ext TP21B.	*a.* Refer to FSM receiver timing diagram (fig. 8). The signal at TP3 is the negative or gate Q17 output shown on figure 8.	*a.* If signal at TP3 is normal and step 1 had an abnormal indication, check 1518327, J15B–J16B. If abnormal perform step 3.
	b. Receiver B	*b.* Channel A TP21C, channel B TP3 on 1518326, J12C–J13C.	*b.* +Ext TP21C.	*b.* Same as *a* above	*b.* Same as *a* above except assembly to be checked is located at J14C–J15C.
3	Same as step 2.				
	a. Receiver A	*a.* Channel A TP21B, channel B TP2 on 1518324, J11B–J12B.	*a.* +Ext TP21B.	*a.* Signal at TP2 is relative square waves that track (same frequency) the input message (TP21B).	*a.* If signal at TP2 is normal and step 2 had an abnormal indication, check 1518326, J13B–J14B. If signal at TP2 is abnormal, check 1518324, J11B–J12B and 1522307, J20B.

	b. Receiver B	*b.* Channel A TP21C, channel B TP2 on 1518324.	*b.* +Ext TP21C.	*b.* Same as *a* above	*b.* Same as *a* above except assemblies to be checked are located at J12C–J13C, J10C–J11C, and J19C.
4	Data and $\overline{\text{data}}$ present but $\overline{\text{ready}}$ $\overline{\text{start}}$ and/or $\overline{\text{remote}}$ $\overline{\text{start}}$ abnormal.			*Note.* Remote start is generated only by the receiver used in the self-test function.	
	a. Receiver A.				
	MFC	Channel A TP18B.	+Ext TP18B.	Positive 3.6-millisecond pulse.	Check 1518325, J17B–J18B. If normal, check 1522348, J19B.
	$\overline{\text{MFC}}$	Channel B TP19B.		Negative 3.6-millisecond pulse.	
	−3v det	Channel A TP24B.	+Ext TP25B.	0v for 4 time slots, then −7.5v for 3 time slots when the ready portion of the sync word is being received. 0v all the time that remote start is being received.	
	+3v det	Channel B TP23B.		0v for 7 time slots, false one time slot, and true one time slot during a sync word. 0v for 4 time slots when a remote start signal is received.	
	b. Receiver B.				
	MFC	Channel A TP18C.	+Ext TP19C.	Same as receiver A	Check 1518325, J16C–J17C. If normal, check 1522348, J18C.
	$\overline{\text{MFC}}$	Channel B TP19C.		Same as receiver A.	
	−3v det	Channel A	+Ext TP25C.	Same as receiver A.	
	+3v det	Channel B		Same as receiver A.	

Step	Symptom	Checkpoint	Sync oscilloscope	Normal indication	Procedure if abnormal indication observed
5	No data PCM rcvr.				
	a. Receiver A	*a.* Oscilloscope channel A TP21B, channel B TP1B.	*a.* +Ext TP21B.	*a.* The signal at TP1B is delayed from the signal at TP21B by 3 to 5 milliseconds.	*a.* If abnormal, check 1518428, J2B–J9B and 1522307, J20B. If normal, check 1518486, J10B.
	b. Receiver B	*b.* Channel A TP21C, channel B TP1C.	*b.* +Ext TP21C.	*b.* Same as receiver A	*b.* If abnormal, check 1518428, J1C–J8C and 1522307, J19C. If normal check 1518486, J9C.
6	No $\overline{\text{data}}$ PCM receiver.				Check 1518486, J10B for receiver A, J9C for receiver B.
7	No ready rcvr.				
	a. Receiver A	*a.* Oscilloscope channel A TP21B, channel B TP2B.	*a.* +Ext TP21B.	*a.* The signal at TP2B follows the 600-cps portion of the signal at TP21B but is delayed by 3 to 5 milliseconds.	*a.* Same as data receiver A.
	b. Receiver B	*b.* Channel A TP21C, channel B TP2C.	*b.* +Ext TP21C.	*b.* Same as receiver A	*b.* Same as data receiver B.
8	No $\overline{\text{Ready}}$ rcvr				Same as $\overline{\text{data}}$ receiver.
9	DCP and IRP not generated.	TP12A	+Ext TP12A.	A train of 6-kc positive clock pulses referenced to −12v and going to Ov.	If abnormal, check 1518493, J13A. If normal, check 593982, J18A for receiver A, J19A for receiver B.
10	DCP not generated	Rcvr A TP9B, rcvr B TP9C.	+Ext TP12A.	Signal is at −12v for four of every 8 CP.	If normal, check 593982, J18A for receiver A, J19A for receiver B. If abnormal, check 1518302, J21B for receiver A, J21C for receiver B.
11	IRP not generated	Same as DCP	Same as DCP	Same as DCP	Same as DCP.
12	Sync data receiver not generated.	Rcvr A TP14B, Rcvr B TP14C.	+Ext TP7B, +Ext TP7C.	A train of negative square wave pulses 167 milliseconds wide and occurring at 750 pps (1.33-millisecond period).	If normal, check 1518302, J21B for receiver A, J21C for receiver B. If abnormal, check 1518303, J20A for receiver A, J21A for receiver B.

Section III. TRANSMITTER SUBFUNCTION TROUBLESHOOTING

79. General

The transmitter subfunction receives data control and ready control signals in digital form and processes these signals to generate a modulated message (either FSM or PCM). The 750-pps T-pulses are also generated in the transmitter subfunction. The troubleshooting chart in paragraph 80 shows the possible symptoms and the probable cause of troubles.

80. FSM Mode Troubleshooting Chart

Step	Symptom	Checkpoint	Sync oscilloscope	Normal indication	Remarks
1	Not transmitting in FSM mode.	*a.* TP24A ground oscilloscope on TP25A.	*a.* +Ext TP17A.	*a.* 1,500-cps sine waves for approx 5 milliseconds followed by approx 4 milliseconds of 1,125-cps sine waves, 1.33 milliseconds of 1,875-cps sine waves, and 1.33 milliseconds of 1,125-cps sine waves. The remainder of the message consists of 1.33-millisecond periods of 1,125 cps for mark and 1,875 cps for space.	*a.* If normal check 1522312, J12A. If no signal, perform step 1*b*.
		b. TP21A	*b.* +Ext TP17A.	*b.* Same as above except signal is attenuated in step 1*a*, depending on switch settings on 1518484, J10A–J11A.	*b.* If normal check 1518484, J10A–J11A. If abnormal, complete step 1*c*.
		c. TP19A	*c.* +Ext TP17A.	*c.* Same as step 1*a* except signal is square waves instead of sine waves.	*c.* If normal check 1518484, J10A–J11A. If abnormal, perform step 1*d*.

		d. TP16A	*d.* Ext TP17A.	*d.* True for ≈9 milliseconds, false for 1.33 millisecond, then true for 1.33 millisecond. Zero volt is the true level and −15 volt is the false level. The remainder of the message consists of 1.33-millisecond periods of 0 volt for true and −15 volt for false.	*d.* If normal check 1518494, J8A and 1518471, J7A. If abnormal check 1518493, J13A.
2	Transmitting continuous 1,500-cps, 1,875-cps, or 1,125-cps sine waves, or not transmitting one of these frequencies.				Check 1518471, J7A and 1518493, J13A.
3	Not generating 750-pps T-pulses.	*a.* TP20A	*a.* +Ext TP17A.	*a.* 1,500-cps square waves	*a.* If abnormal check 1518494, J9A and 1518471, J7A.
		b. TP3A	*b.* +Ext TP17A.	*b.* 1,500-cps square waves	*b.* If abnormal check 1522312, J12A. If normal check 1518493, J13A.

81. PCM Mode Troubleshooting Chart

Step	Symptom	Checkpoint	Sync oscilloscope	Normal indication	Remarks
1	Not transmitting in PCM mode.	*a.* J12A–Y		*a.* —26.5 vdc	*a.* If abnormal, see TM 11–5840–273–30.
		b. TP22A, ground oscilloscope at TP23A.	*b.* +Ext TP17A.	*b.* Approximately 5-volt peak-to-peak sine waves of 1,500 cps combine with a 600-cps sine wave for 4 milliseconds. Remainder of message consists of bursts of 1,500 cps.	*b.* If normal check 1522312, J12A. If no signal check 549591, J14A–J17A. If 600-cps portion of signal is not present, perform step 2. If this portion of signal is present, perform step 3.
2	Not transmitting 600-cps portion of message.				Check 549591, J14A–J17A.
3	Not transmitting 1,500-cps portion of message.	TP4A	+Ext TP17A.	1,500-cps sine waves for approx 8 milliseconds and then 1.33 millisecond of no signal followed by remainder of message in bursts of 1,500 cps.	If abnormal check 1522312, J12A. If normal perform step 4.
4	Not generating 750-pps T-pulses.	*a.* TP21A	*a.* —Ext TP17A.	*a.* Continuous 1,500-cps sine waves.	*a.* If normal check 1522312, J12A. If abnormal, perform step *b* below.
		b. TP20A	*b.* +Ext TP17A.	*b.* Continuous 1,500-cps square waves.	*b.* If normal check 1518484, J10A–J11A and 1522312, J12A. If abnormal check 1518594, J9A and 1518471, J7A.

CHAPTER 8

REMOVAL AND REPLACEMENT OF PARTS

82. General

This chapter covers the procedures required for the removal and replacement of the transmitter-receiver digital drawer and mechanical assemblies within the unit.

a. Tools Required. To perform the removal and replacement procedures, the following handtools, contained in Tool Kit TK,-105/MSQ-28, are required:

(1) Two standard screwdrivers; one each large and small.
(2) Three Phillips screwdrivers; one each large, small, and stubby.
(3) Long-nosed pliers.
(4) Adjustable crescent wrench.
(5) Light hammer.
(6) Set of Allen wrenches.
(7) Flashlight.

b. Preliminary Instructions. When performing the removal procedures, keep careful track of all screws, nuts, bolts, and other removed parts. When possible, place all small parts in a suitable container as they are removed to facilitate the reassembly of the component concerned.

Warning: **Before performing any particular operation, make sure that the power to the equipment is removed.**

83. Removal and Replacement of Unit Drawer

The transmitter-receiver drawer is typical of other unit drawers found in the RDPC and WMC. Refer to TM 11-5840-271-30/18 or TM 11-5840-272-30/17 for removal and replacement procedures for the drawer.

84. Removal and Replacement of Card Assemblies

a. General. There are two types of card assemblies: I-frame and H-frame. The removal and replacement procedures are identical for both types.

b. Removal and Replacement. The procedures for removal and replacement of card assemblies are contained in TM 11-5840-271-30/18 or TM 11-5840-272-30/17.

CHAPTER 9

ALIGNMENT AND ADJUSTMENT

85. General

This chapter provides procedures for the alignment and adjustment of the transmitter-receiver. All procedures are performed under dynamic conditions to provide the necessary inputs to the transmitter-receiver.

86. Tools and Test Equipment Required

a. The following chart lists the test equipment required and its use to align and adjust the transmitter-receiver.

Test equipment	Manual	Use
Oscilloscope AN/USM-81	TM 11-6625-219-12	Waveform observations.
Multimeter AN/URM-105	TM 11-6625-203-12	Voltage measurements.

b. The tools required to align and adjust the transmitter-receiver are contained in Tool Kit TK-105/MSQ-28.

87. FSM Receiver Adjustments

a. Balance Control R33. Resistor R33 is a screwdriver adjustment located on assembly 1518325. Resistor R33 is adjusted so that the notch on the waveform at TP2 occurs at two-thirds of the maximum amplitude. (See fig. 33①.)

b. Voltage Level Control R6. Resistor R6 is a screwdriver adjustment located on assembly 1518327. Resistor R6 is adjusted for 0 volt at TP1 on 1518325 when 1,500 cps is present in the incoming FSM message.

88. PCM Receiver Adjustments

a. MESSAGE LEVEL Adjust R1. Resistor R1 is a screwdriver adjustment located in 1518428. With a PCM message applied, and AGC-DISABLE switch in the DISABLE position, adjust R1 for −1.35 volt ±0.4 volt at TP1 and −1.15 volt ±0.4 volt at TP2 on 1518428.

b. AGC Adjust R12. Resistor R12 is a screwdriver adjustment located on assembly 1518428. Set AGC-DISABLE switch to the AGC position and adjust R12 for −1.35 volt +0.4 volt at TPB2 and −1.15 volt ±0.4 volt at TPB1 with the same input applied as in *a* above.

c. Slicer Adjust R4, and R30. Resistors R4 and R30 are screwdriver adjustments located on 1518486.

(1) *Slicer adjust R4.* Resistor R4 adjusts the proper width of the smoothed data signal by varying the bias level of Q1. With −1.35 volt ±0.4 volt dc applied at TPB1, adjust R4 for a 0- to −6-volt signal at TPB2 and TPB3 on 1518428. When TPB2 is at 0 volt, TPB3 is at −6 volts.

(2) *Slicer adjust R30.* Resistor R30 adjusts the width of the smoothed ready signal by varying the bias level for Q8. With −1.35 volt ±0.4 volt dc applied at TPB4, adjust R30 for a 0- to −6-volt signal at TPB5 and TPB6 on 1518428. When TPB5 is at 0 volt, TPB6 is at −6 volts.

89. FSM Transmitter Adjustments

There are no adjustments required for FSM transmitter operation.

90. PCM Transmitter Adjustments

a. Level Control R5. Level control R5 located on 1522312, J12A is a screwdriver adjustment that is used to set the level of the 1,500-cps data modulated signal. Observe the signal at TP4A and adjust R5 for 12 volts ±0.1 volt peak-to-peak when data is present in the message.

b. AMPL ADJ R6, 600 CPS. Resistor R6 is a screwdriver adjustment located on 549591, J14A–J17A. With a true signal applied at TP17A adjust R6 for a signal of 5.5 volts ±0.5 volt at TP22A.

91. Power Supply Adjustments

a. Plus 12-Volt Power Supply. Voltage adjust control R12 located on 1512530, J1A–J5A adjusts the +12-volt power supply output. Resistor R12 is a screwdriver adjustment. Observe the signal at TP29A and adjust R12 for +12 volts.

b. Minus 12-Volt Power Supply. Voltage adjust control R12 located on 1512552, J6A adjusts the −12-volt power supply output. Observe the signal at TP30A and adjust R12 for −12 volts.

APPENDIX

REFERENCES

Following is a list of references applicable to this manual and available to the DS maintenance personnel:

DA Pam 310-4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (types 4, 6, 7, 8, and 9), Supply Catalogs (type CL), Supply Bulletins Lubrication Orders, and Modification Work Orders
MIL-STD 17	Mechanical Symbols
TM 9-213	Painting Instructions for Field Use
TM 11-690	Basic Theory and Application of Transistors
TM 11-4940-205-10	Operator's Manual: Electronic Shop, Semitrailer Mounted AN/MSM-34
(C) TM 11-5840-271-30/1	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B, Description, Data, and General Functional Theory (U)
(C) TM 11-5840-271-30/2	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; Data Exchange Functional Theory and Troubleshooting (U)
(C) TM 11-5840-271-30/3	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B, Timing and Storage Functions, Theory and Troubleshooting (U)
(C) TM 11-5840-271-30/4	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B, Extrapolation Function Analysis and Troubleshooting (U)
(C) TM 11-5840-271-30/5	Field (Third Echelon) Maintenance Manual: Processing Center Radar Data OA-4333/MSQ-28B, Radar Data Conversion Function, Theory and Troubleshooting (U)
(C) TM 11-5840-271-30/6	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B, Track Simulation Function, Theory and Troubleshooting (U)
(C) TM 11-5840-271-30/7	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B, ARDME Function, Theory and Troubleshooting (U)
(C) TM 11-5840-271-30/8	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B, Tracking Computer Function Theory (U)
(C) TM 11-5840-271-30/9	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B, Tracking Computer Function, Troubleshooting (U)
TM 11-5840-271-30/10	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B, Tracking Computer Test and Digital Data Display Functions, Theory, and Troubleshooting

(C) TM 11-5840-271-30/11	DS Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B, Radar Information Processing Function, Theory and Troubleshooting (U)
(C) TM 11-5840-271-30/12	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B, Consoles Display Generation Function, Theory and Troubleshooting (U)
(C) TM 11-5840-271-30/13	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; DT Consoles Received Information Function, Theory and Troubleshooting (U)
(C) TM 11-5840-271-30/14	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; RHI Consoles Received Information Function, Theory and Troubleshooting (U)
(C) TM 11-5840-271-30/15	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; DT Consoles Data Entry Function, Theory and Troubleshooting (U)
(C) TM 11-5840-271-30/16	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; RHI Consoles Data Entry Function, Theory and Troubleshooting (U)
TM 11-5840-271-30/17	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; Voice Communications and State of Alert Function, Theory and Troubleshooting
(C) TM 11-5840-271-30/18	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; Subsystem Maintenance Information (U)
(C) TM 11-5840-271-30/19/1; (C) TM 11-5840-271-30/19/2	Direct Support Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; Unit Schematic Diagrams (Parts 1 and 2) (U)
(C) TM 11-5840-271-30/20/1; (C) TM 11-3950-271-30/20/2; (C) TM 11-5840-271-30/20/3	Direct Support Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; Card Assembly Schematic Diagrams (Parts 1, 2, and 3) (U)
TM 11-5840-271-30/21	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; Detailed Circuit Theory
(C) TM 11-5840-271-30/22	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B; Component Location, Removal and Replacement, and Voltage and Resistance Data (U)
(C) TM 11-5840-272-30/1	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Description, Data, and General Functional Theory (U)
(C) TM 11-5840-272-30/2	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Local Input Buffer and Data Controls Function, Theory and Troubleshooting (U)
(C) TM 11-5840-272-30/3	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Remote Input Buffers Function, Theory and Troubleshooting (U)
(C) TM 11-5840-272-30/4	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Remote Data Controls Function, Theory and Troubleshooting (U)
(C) TM 11-5840-272-30/5	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Timing and Storage Functions, Theory and Troubleshooting (U)

(C) TM 11-5840-272-30/6	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B and OA-4972/MSQ-56; Extrapolation Function, Analysis and Troubleshooting (U)
(C) TM 11-5840-272-30/7	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Weapons Display Control Function, Theory and Troubleshooting (U)
(C) TM 11-5840-272-30/8	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Weapons Monitoring Console Display Function, Theory and Troubleshooting (U)
(C) TM 11-5840-272-30/9	DS Maintenance Manual: Weapons Monitoring Centers OA-4342/MSQ-28B and OA-4972/MSQ-56; BN/BTRY ADL Sequencer Functions (U)
(C) TM 11-5840-272-30/10	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; BN/BTRY ADL Input-Output-Buffer Function, Theory and Troubleshooting (U)
(C) TM 11-5840-272-30/11	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Weapons Monitoring Console Controls and Track Number Readout Functions, Theory and Troubleshooting (U)
(C) TM 11-5840-272-30/12	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; BN/BTRY ADL Data Control Function, Theory and Troubleshooting (U)
(C) TM 11-5840-272-30/13	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Local Output Buffer Function, Theory and Troubleshooting (U)
(C) TM 11-5840-272-30/14	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Remote Output Buffer Function, Theory and Troubleshooting (U)
TM 11-5840-272-30/15	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Voice Communications and State of Alert Function, Theory and Troubleshooting
(C) TM 11-5840-272-30/16	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Self Test Function, Theory and Troubleshooting (U)
(C) TM 11-5840-272-30/17	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Subsystem Maintenance Information (U)
(C) TM 11-5840-272-30/18/1; (C) TM 11-5840-272-30/18/2; (C) TM 11-5840-272-30/18/3	DS Maintenance Manual: Weapons Monitoring Centers OA-4342/MSQ-28B and OA-4972/MSQ-56; Unit Schematic Diagrams (Parts 1, 2, and 3) (U)
(C) TM 11-5840-272-30/19/1; (C) TM 11-5840-272-30/19/2; (C) TM 11-5840-272-30/19/3	DS Maintenance Manual: Weapons Monitoring Centers OA-4342/MSQ-28B and OA-4972/MSQ-56; Card Assembly Schematic Diagrams (Parts 1, 2, and 3) (U)
TM 11-5840-272-30/20	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Detailed Circuit Theory
(C) TM 11-5840-272-30/21	Field (Third Echelon) Maintenance Manual: Weapons Monitoring Center OA-4342/MSQ-28B; Component Location, Removal and Replacement, and Resistance Data (U)

TM 11-5840-273-30	Field (Third Echelon) Maintenance Manual: Processing Center, Radar Data OA-4333/MSQ-28B and Weapons Monitoring Center OA-4342/MSQ-28B; Power Supplies and Power Control Panels
TM 11-5895-264-25	Basic Circuit Theory for Antiaircraft Defense System AN/MSQ-4
(C) TM 11-5895-292-10	Operators Manual: Antiaircraft Defense System AN/MSG-4 (U)
(C) TM 11-5895-292-23	Organizational and Field (Third Echelon) Maintenance Manual: Antiaircraft Defense System AN/MSG-4 (U)
TM 11-6625-203-12	Operators and Organizational Maintenance Manual: Multimeter AN/URM-105, including Multimeter ME-77/U
TM 11-6625-219-12	Operators and Organizational Maintenance Manual: Oscilloscope AN/USM-81
TM 11-6625-430-12	Operators and Organizational Maintenance Manual: Test Set, Electronic Circuit Plug-in Unit TS-1712/MSQ-28
TM 11-6625-432-12	Operators and Organizational Maintenance Manual: Test Set, Electronic Circuit Plug-in Unit TS-1686/MSM-34
TM 38-750	Army Equipment Record Procedures

GLOSSARY

Section I. ABBREVIATIONS

AADCP	Army Air Defense Command Post
ADL	Automatic data link
BBD	Base-band data
bit	binary digit
CCI	Central control indicator
CP	Clock pulse
DCP	Delayed clock pulse
DREV	Drum revolution
ext	external
FSM	Frequency shift modulation
int	internal
IRP	Input ready pulse
lc	inductance-capacitance (network)
K	1,000 ohms
kpps	thousand pulses per second
LSD	Least significant digit
MFC	Midfrequency control
MOD	Modulo
MS	Mark signal
MSD	Most significant digit
PCM	Pulse code modulation
rc	resistance-capacitance (network)
RDPC	Radar data processing center
RTC	Ready tone control
WMC	Weapons monitoring center

Section II. DEFINITIONS OF UNUSUAL TERMS

ADL Message—Digital data indicated by the presence or absence of an assigned frequency or by the presence of one of three different, distinct frequencies that is divided into either five or eight words that contain track coordinate, velocity, and auxiliary information.

AN/MSG-4 System—An Army air defense fire distribution system.

Army Air Defense Command Post—Operations Central AN/MSQ-28B or AN/MSQ-56. The highest level at which tactical integration of the various weapons associated with an AN/MSG-4 System takes place, and which is situated at the Air Defense Artillery Group.

Automatic Data Link—Communication lines through which digital data of the ADL messages are transmitted and received automatically.

Binary Data—Information expressed in either of two states (0 or 1, true of false, etc.).

Data Time Slot—A 1.33-millisecond time interval coincident with each digit of sync data.

Delayed Clock Pulse—A −6-volt pulse occurring at the center of each data time slot. The delayed clock pulse is generated by the receiver synchronizer subfunction and supplied to the input buffer. The input buffer uses it with subsystem timing circuits to synchronize the data to subsystem timing.

Function—A portion of Operations Central AN/MSQ-28B or AN/MSQ-56 which performs a specific operation. Division into functions is based on electrical and electronic characteristics, rather than on the physical packaging of the components.

Input Ready Pulse—A −6-volt pulse occurring during the sync word of each message. The input ready pulse is generated by the receiver synchronizer subfunction and supplied to the input buffer. The input buffer uses it to establish initial logic conditions necessary for message processing.

Mark—A true data bit. Used here in conjunction with FSM mode and containing an 1,125-cps signal.

a. (PCM)

Message Frame—A configuration of 1,500-cps and 600-cps signals used to indicate the binary data concerning one track transmitted throughout the AN/MSG-4 System.

b. (FSM) A configuration of 1,125-cps, 1,500-cps, and 1,875-cps signals used to indicate the binary data concerning one track transmitted throughout the AN/MSG-4 System.

Message Time Slot—A 1.33-millisecond time interval coincident with each digit in the message frame.

Radar Data Processing Center—A digital and radar data processing and display subsystem that is part of Operations Central AN/MSQ–28B or AN/MSQ–56.

Remote Stations—Other AADCP's or AN/MSG–4 System complexes which communicate with the local AN/MSG–4 System.

Space—A false data bit. Used here in conjunction with FSM mode and containing an 1,875-cps signal.

Sync Data—The digital data output of the receiver.

Sync Digit—Message time slot 7. The sync digit always contains 2 cycles of 1,500-cps signal in PCM or 1½ cycles of 1,125-cps signal in FSM.

Sync Guard—Message time slot 6. The sync guard never contains 1,500-cps signal.

Sync Word—The first word of all message frames and is used to establish the automatic gain control levels of the participating receivers and to synchronize the receiving stations timing circuits with the entering message frame.

Track—All radar returns from airborne vehicles and markers displayed on the consoles of Operations Central AN/MSQ–28B or AN/MSQ–56.

Weapons Monitoring Center—A digital data processing, display, and fire control subsystem that is part of Operations Central AN/MSQ–28B or AN/MSQ–56.

Word—A binary expression of related intelligence.

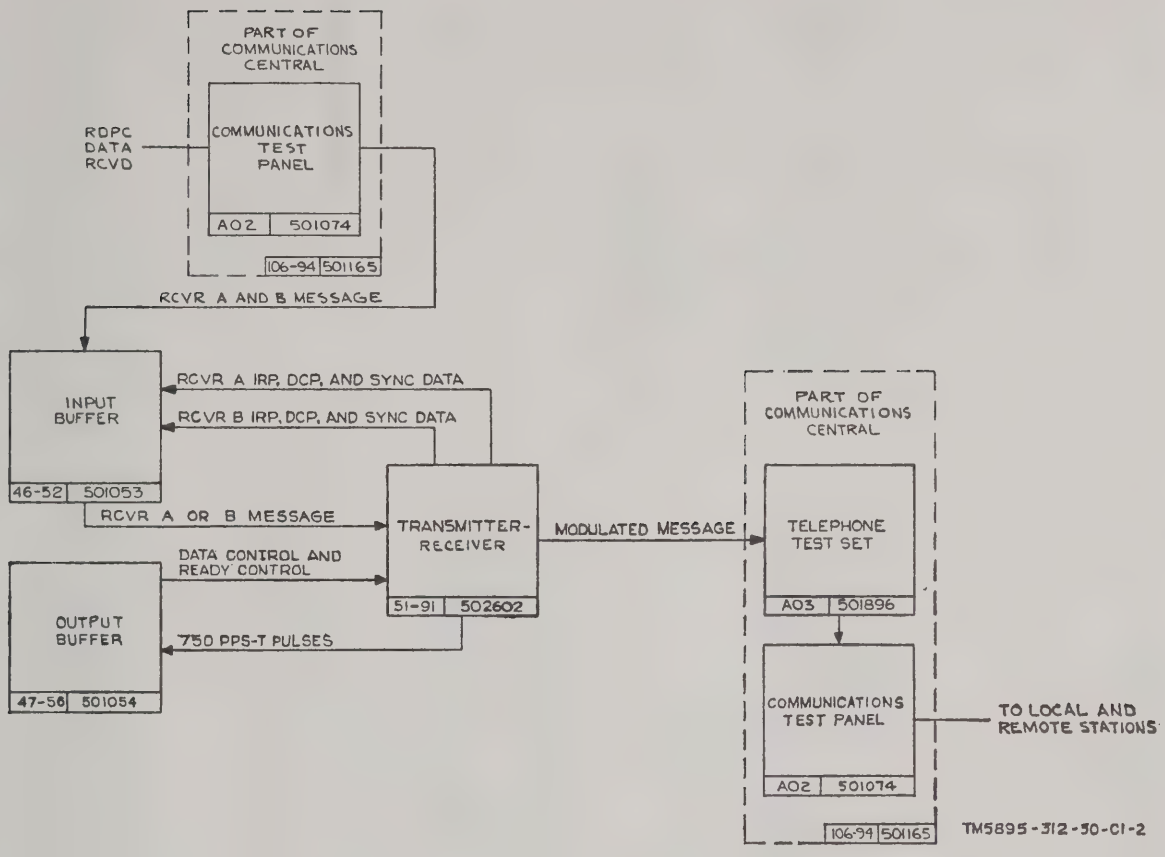


Figure 1. RDCP transmitter-receiver data flow, block diagram.

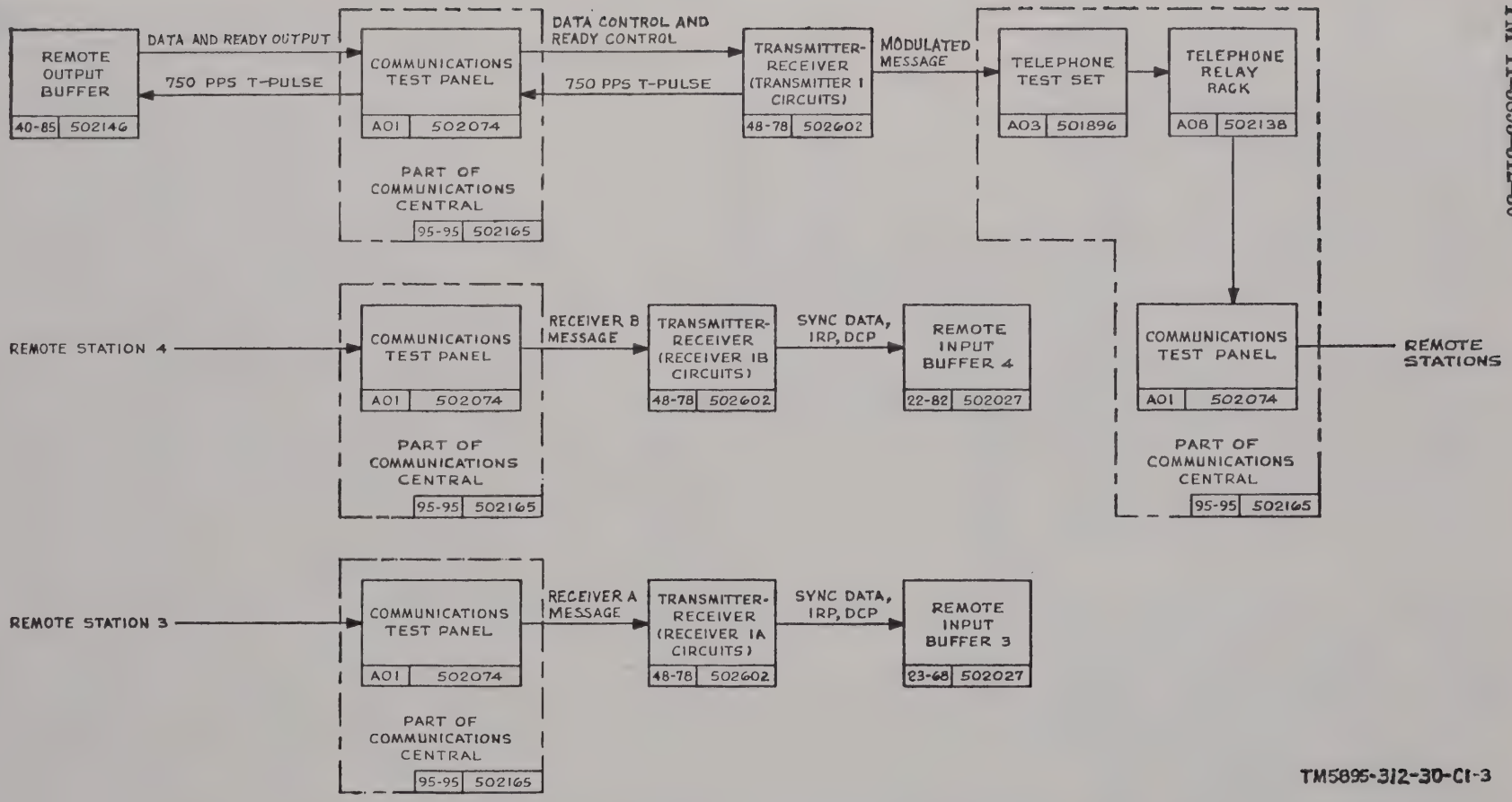


Figure 2. WMC transmitter-receiver 1, data flow, block diagram.

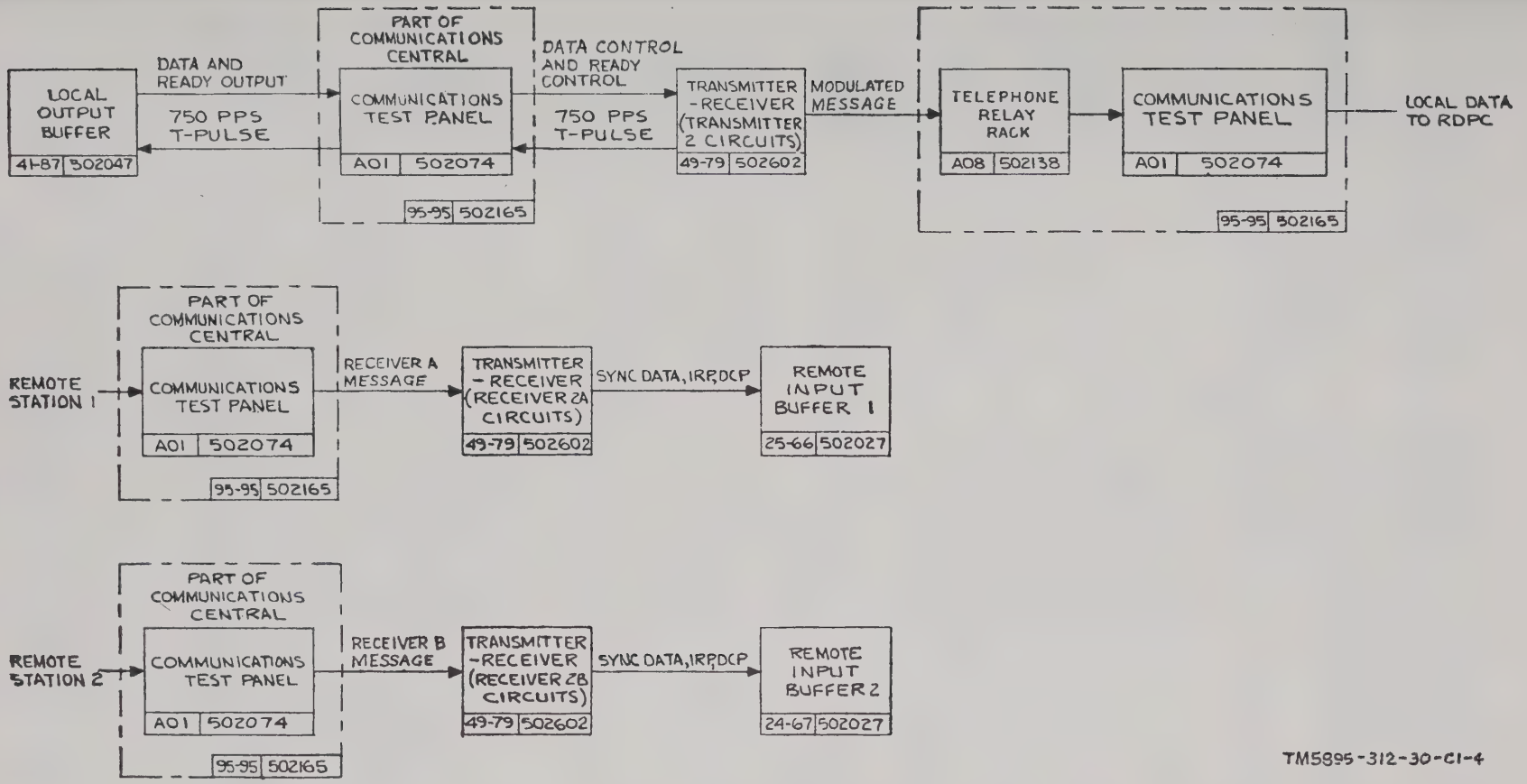


Figure 3. WMC transmitter-receiver 2, data flow, block diagram.

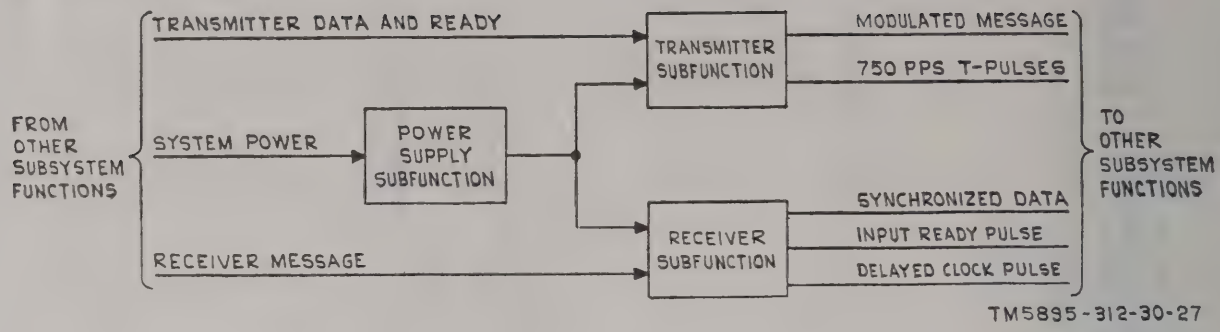


Figure 5. Transmitter-receiver, block diagram.

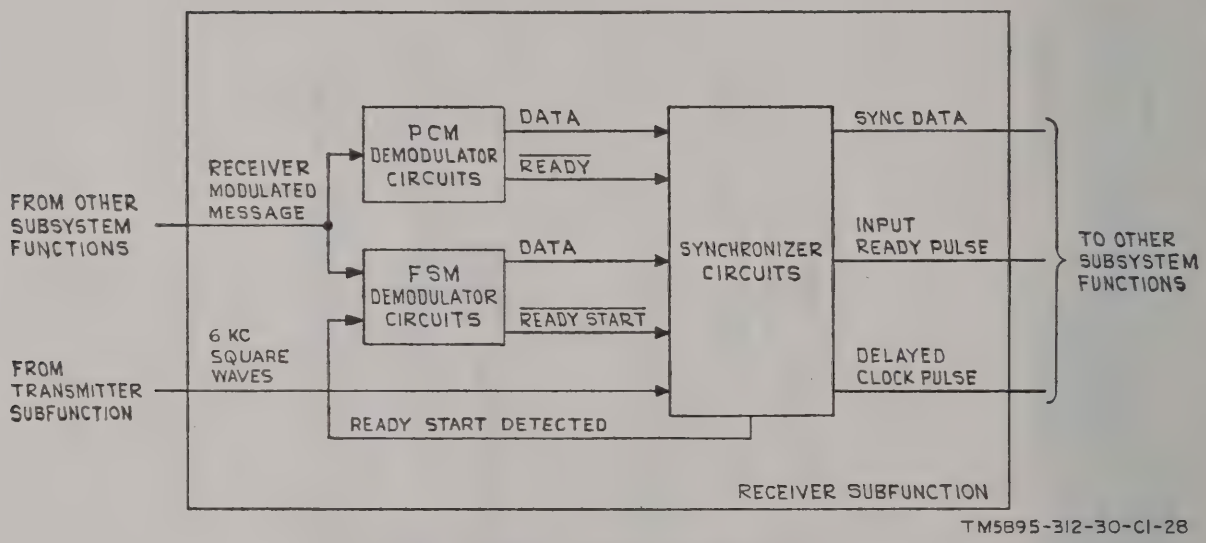


Figure 6. Receiver-subfunction, block diagram.

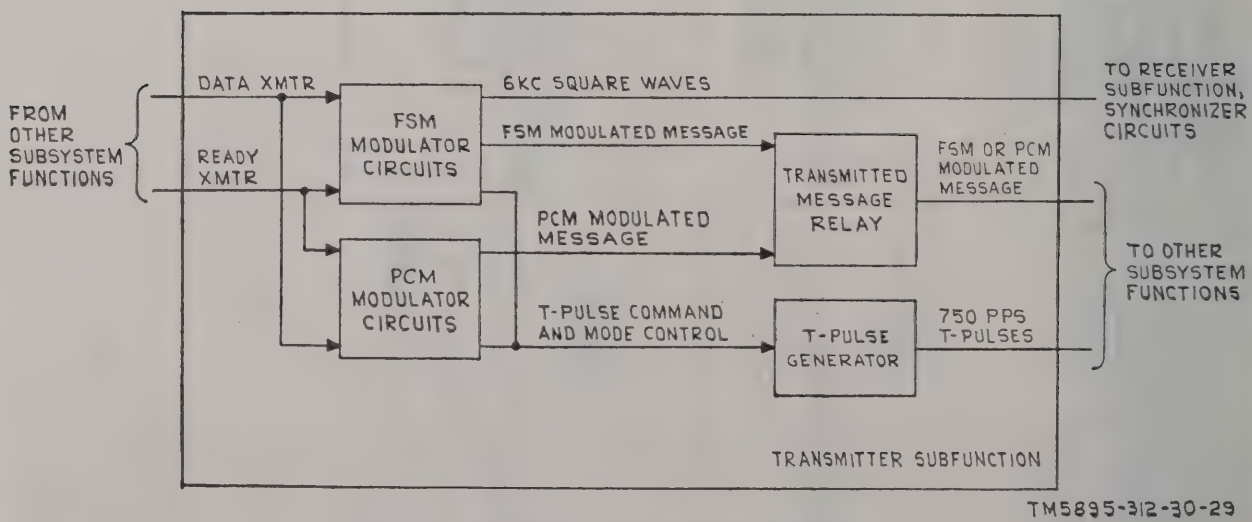


Figure 7. Transmitter subfunction, block diagram.

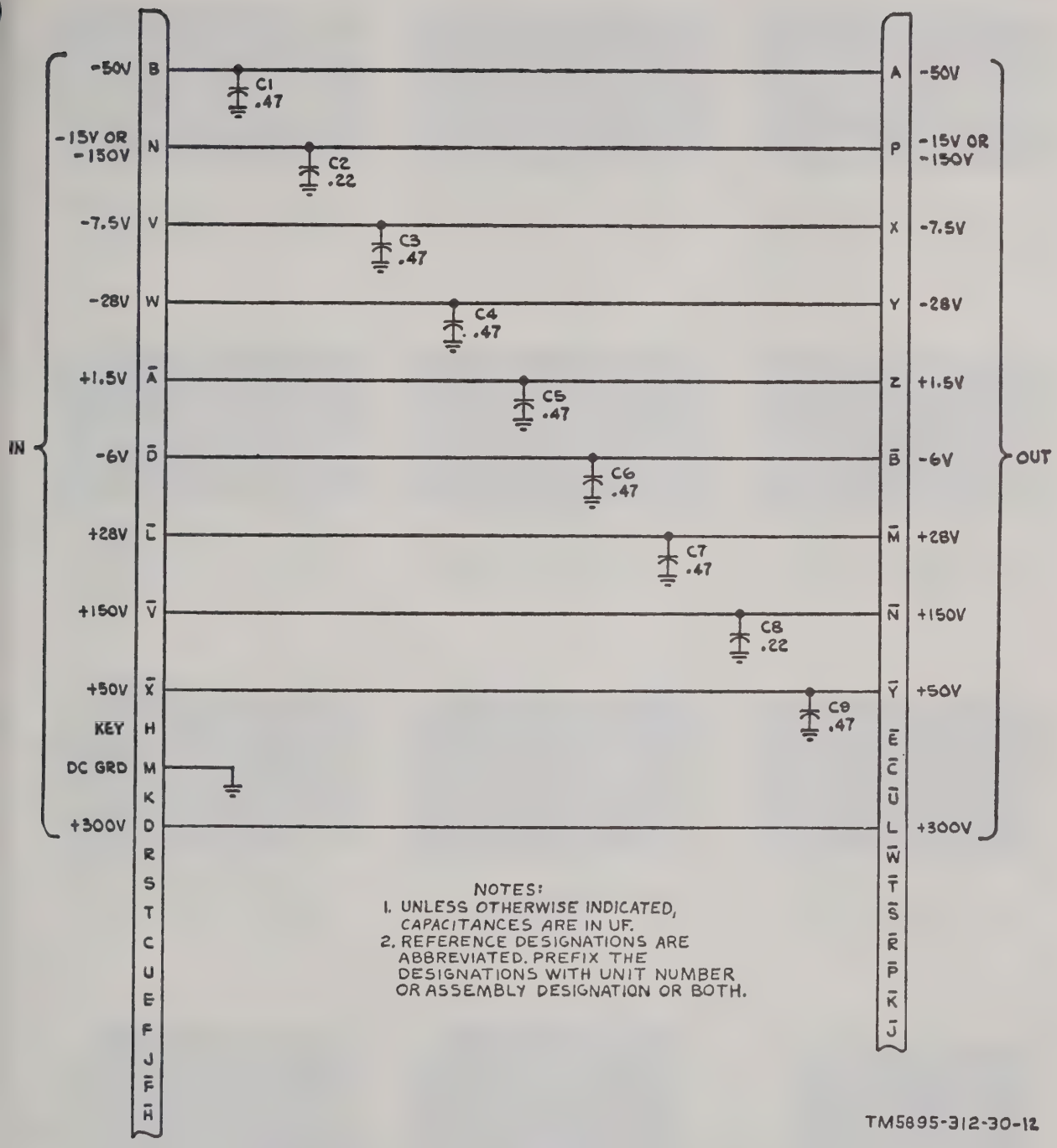
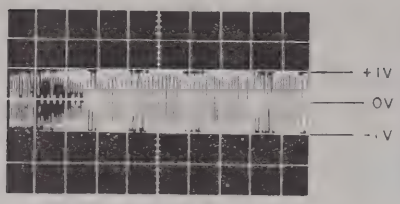
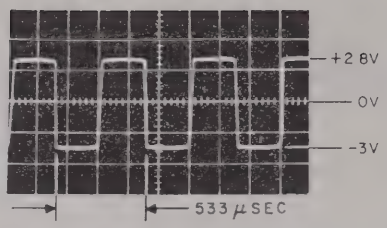


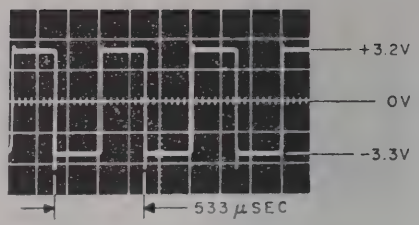
Figure 13. Direct current power filter 547885, schematic diagram.



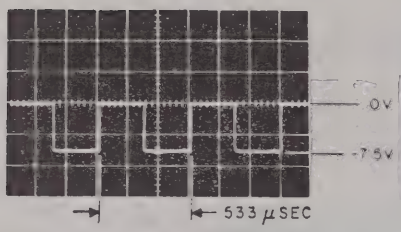
A TYPICAL FSM MESSAGE AT TP1 OF ASSEMBLY 1518324 SYNC+INT 1V/DIV 10 MSEC/DIV



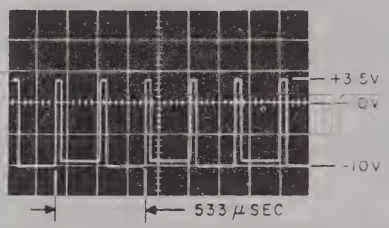
B FILTERED DATA (FSM) AT TP2 OF 1518324 2V/DIV 175 μ SEC/DIV SYNC+INT



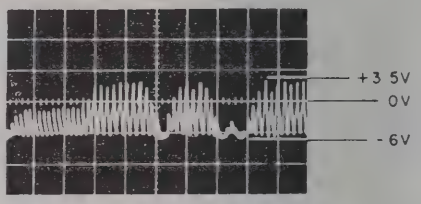
C EMITTER FOLLOWER Q10 OUTPUT AT TP2 ON 1518326 2V/DIV 175 μ SEC/DIV SYNC+INT



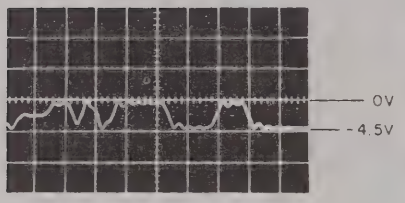
D SQUARING AMPLIFIER OUTPUT AT TP1 ON 1518326 175 μ SEC/DIV SYNC+INT 5V/DIV



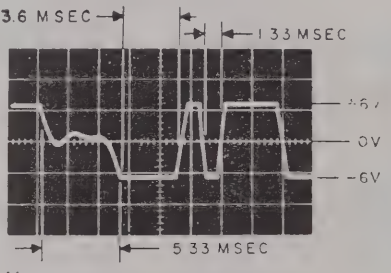
E LIMITED DATA (FSM) AT TP3 ON 1518326 5V/DIV 175 μ SEC/DIV SYNC+INT



F DIODE BRIDGE OUTPUT AT TP2 ON 1518327 5V/DIV 2MSEC/DIV SYNC+INT

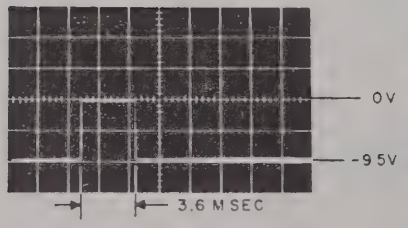


G LOW PASS FILTER FL1 OUTPUT AT TP3 ON 1518327 5V/DIV 2MSEC/DIV SYNC+EXT AT TP1 ON 1518324

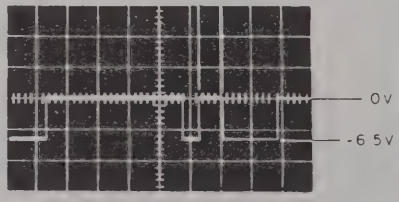


H BBD AT TP1 ON 1518325 5V/DIV 2MSEC/DIV SYNC+INT

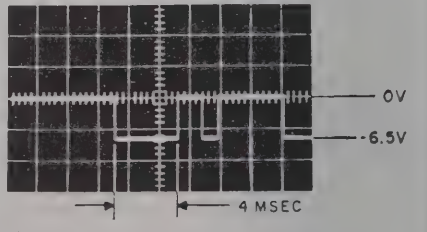
J MFC SWITCH Q6 INPUT AT TP2 ON 1518325 2V/DIV 2MSEC/DIV SYNC+EXT AT TP1 ON 1518324



K MFC AT TP3 ON 1518325 5V/DIV 2MSEC/DIV SYNC+EXT AT TP1 ON 1518324



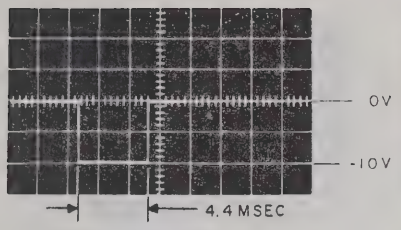
L INVERTER Q8 OUTPUT AT J17B-J ON 1518325 5V/DIV 2MSEC/DIV SYNC+EXT AT TP1 ON 1518324



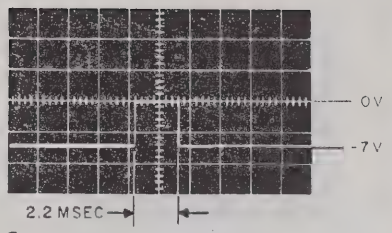
M INVERTER Q13 OUTPUT AT J17B-V ON 1518325 5V/DIV 2MSEC/DIV SYNC+EXT AT TP1 ON 1518324

TM5895-312-30-CI-54 ①

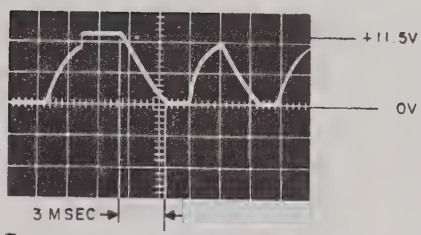
Figure 33①. FSM waveforms (part 1 of 2).



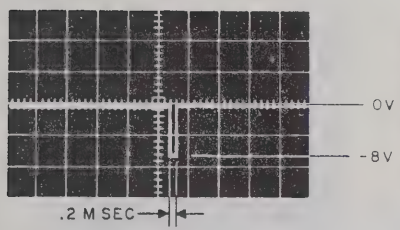
N INVERTER Q7 OUTPUT AT
J17B-W ON 1518325
J8-W 5V/DIV 2MSEC/DIV
SYNC+EXT AT TP1 ON 1518325



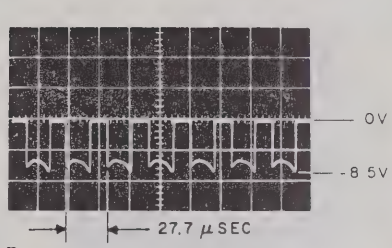
O INVERTER Q3 OUTPUT AT
TP1 ON 1522348
5V/DIV 2MSEC/DIV
SYNC+EXT AT TP1 ON 1518325



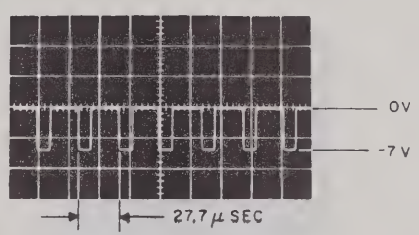
P READY START SWITCH Q11
INPUT AT TP4 ON 1522348
5V/DIV 2MSEC/DIV
SYNC+EXT AT TP1 ON 1518325



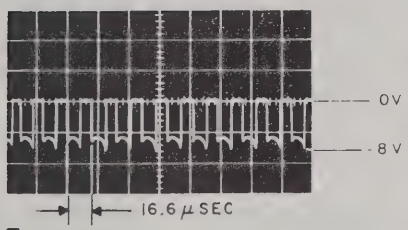
Q $\overline{\text{READY START}}$ OUTPUT AT
TP2 ON 1522348
5V/DIV 2MSEC/DIV SYNC-EXT
AT TP3 ON 1518325



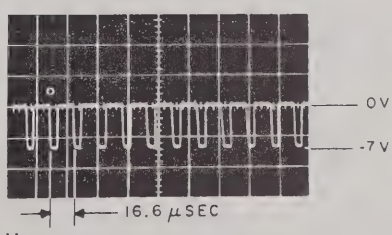
R 36-KC OSCILLATOR OUTPUT AT
TP1 ON 1518471 5V/DIV
20μSEC/DIV SYNC+INT



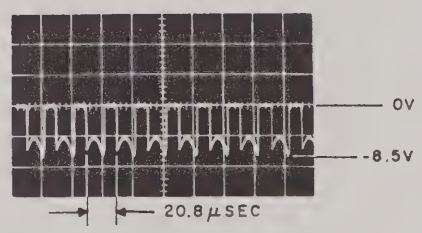
S MARK AND GATE OUTPUT
AT TP2 ON 1518471 5V/DIV
20μSEC/DIV 5V/DIV SYNC+INT



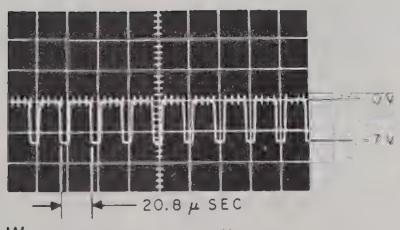
T 60-KC OSCILLATOR OUTPUT
AT TP3 ON 1518471
5V/DIV 20μSEC/DIV SYNC + INT



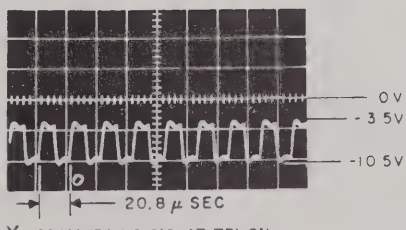
U SPACE AND GATE OUTPUT AT
TP5 ON 1518471 5V/DIV
20μSEC/DIV SYNC+INT



V 48-KC OSCILLATOR OUTPUT
AT TP7 ON 1518471 5V/DIV
20μSEC/DIV SYNC+INT



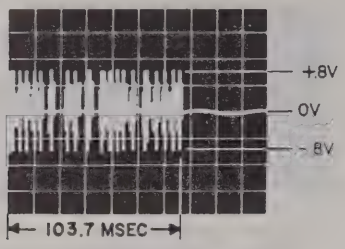
W MID FREQUENCY AND GATE
OUTPUT AT TP6 ON 1518471
5V/DIV 20μSEC/DIV SYNC+INT



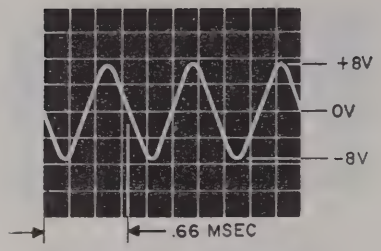
X 60/48/36-KC SIG. AT TP1 ON
1518494 (WHEN MID FREQUENCY
SIGNAL IS PRESENT) 5V/DIV
20μSEC/DIV SYNC+INT

TM5895-312-30-CI-54②

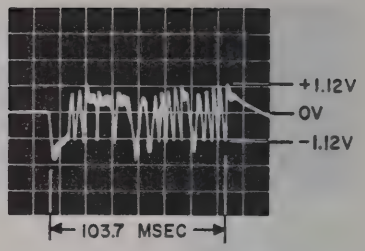
Figure 33②. FSM waveforms (part 2 of 2).



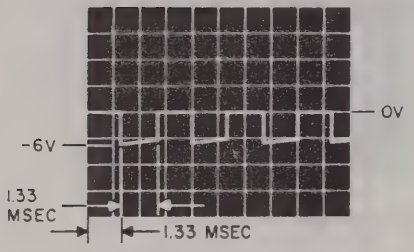
A TYPICAL PCM MESSAGE AT TP4 ON 549591, J14A-J17A SYNC-EXT AT TP1 ON 549591, J14A-J17A 15 MSEC/DIV .5V/DIV



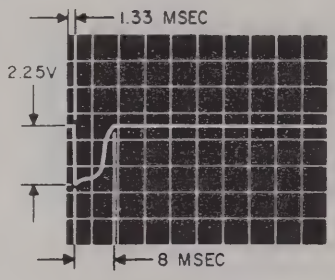
B 1,500-CPS DATA MODULATED AT TP4 ON 549591, J14A-J17A SYNC-EXT AT TP1 ON 549591, J14A-J17A .2 MSEC/DIV 5V/DIV



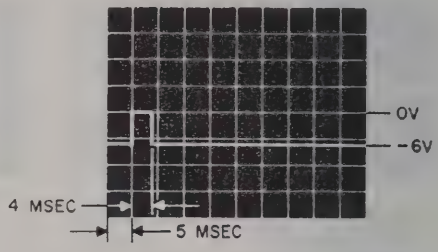
C SMOOTHED DATA AT TPB-1 ON 1518486 15 MSEC/DIV 1V/DIV AC ONLY SYNC-EXT AT TP3 ON 1518428



D PCM DATA OUTPUT OF 1,500-CPS SCHMIDT TRIGGER SHAPER AT TPB-3 ON 1518486 1 MSEC/DIV 5V/DIV SYNC+EXT AT TPB-1 ON 1518486



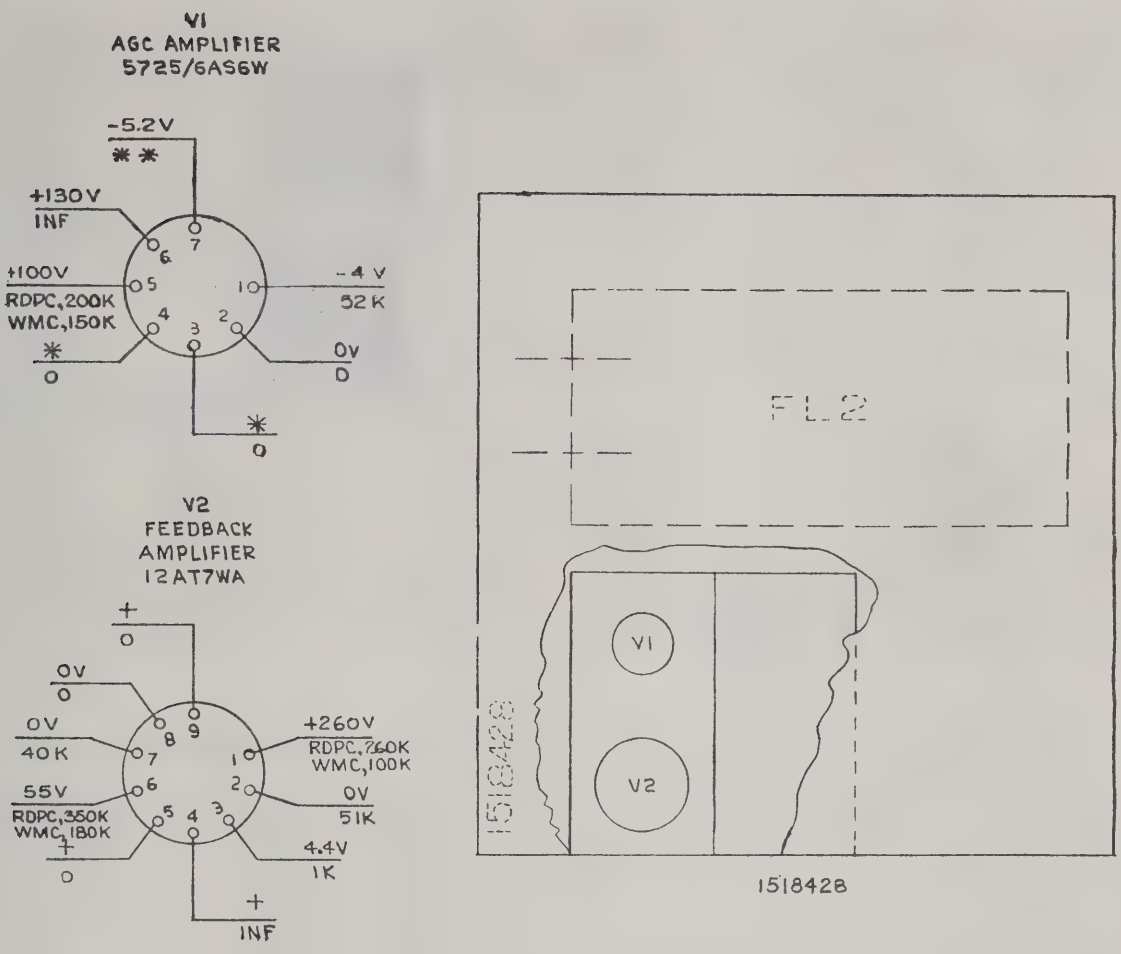
E SMOOTHED READY AT TPB-4 ON 1518486 5 MSEC/DIV 1V/DIV (AC INPUT) SYNC -EXT AT TP3 ON 1518428



F OUTPUT OF 600-CPS SCHMIDT TRIGGER SHAPER AT TPB-2 ON 1518428 5 MSEC/DIV 5V/DIV SYNC -EXT AT TP3 ON 1518428

TM5895-312-30-55

Figure 34. PCM waveforms.



NOTES:

1. 115V AC INPUT
2. DC VOLTAGES AND RESISTANCES MEASURED TO DC GROUND WITH A 20,000 OHMS-PER-VOLT METER.
3. VOLTAGE READINGS ABOVE LINE, RESISTANCE READINGS BELOW LINE. K DENOTES THOUSAND, MEG DENOTES MILLION, INF DENOTES INFINITY.
4. * INDICATES 6.3V AC BETWEEN PINS SO MARKED.
5. + INDICATES 6.3V AC BETWEEN PIN 9, AND PIN 4 OR 5.
6. S1 IN [AGC] POSITION.
7. R12 AND R1 FULLY CW.
8. * * DEPENDS ON POLARITY. METER READS EITHER 2K OR 6.8M.

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Figure 35. Transmitter-receiver 502602, vacuum tube voltage and resistance diagram.

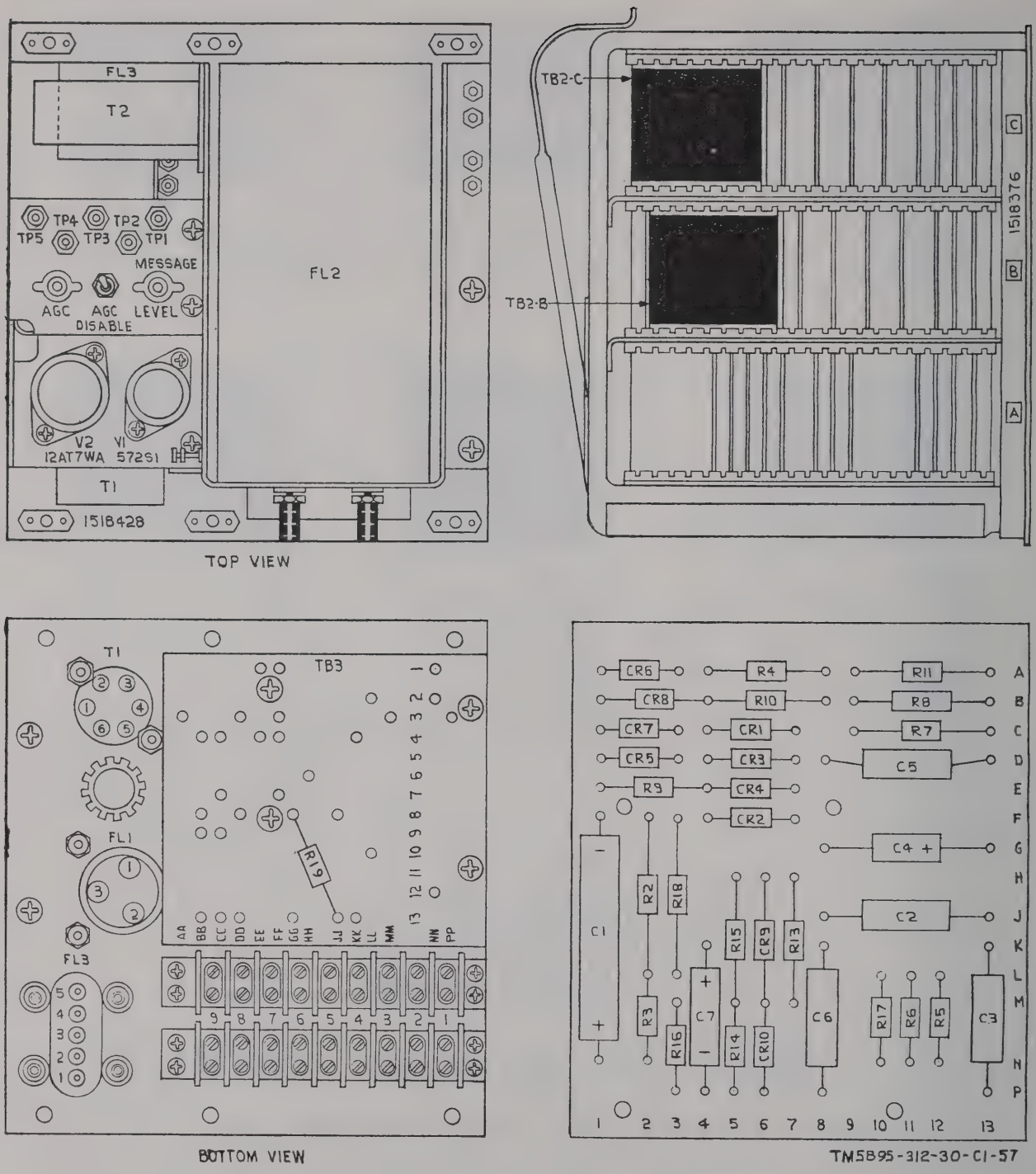

Figure 36. Amplifier demodulator chassis, parts location diagram.

By Order of the Secretary of the Army:

HAROLD K. JOHNSON,
General, United States Army,
Chief of Staff.

Official:

J. C. LAMBERT,
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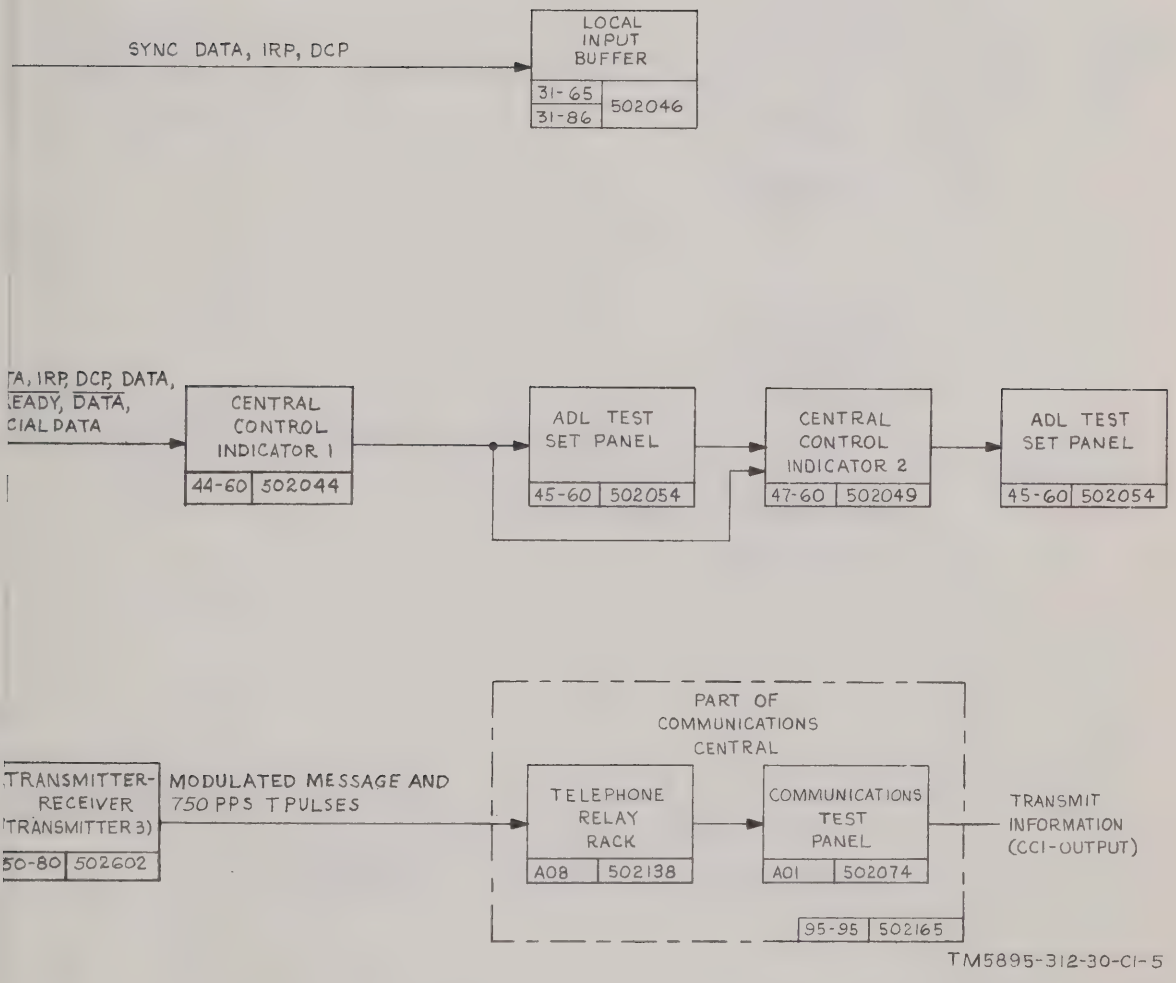


eceiver 3, data flow, block diagram.

761-494 O - 65 Fols. Text No. 1

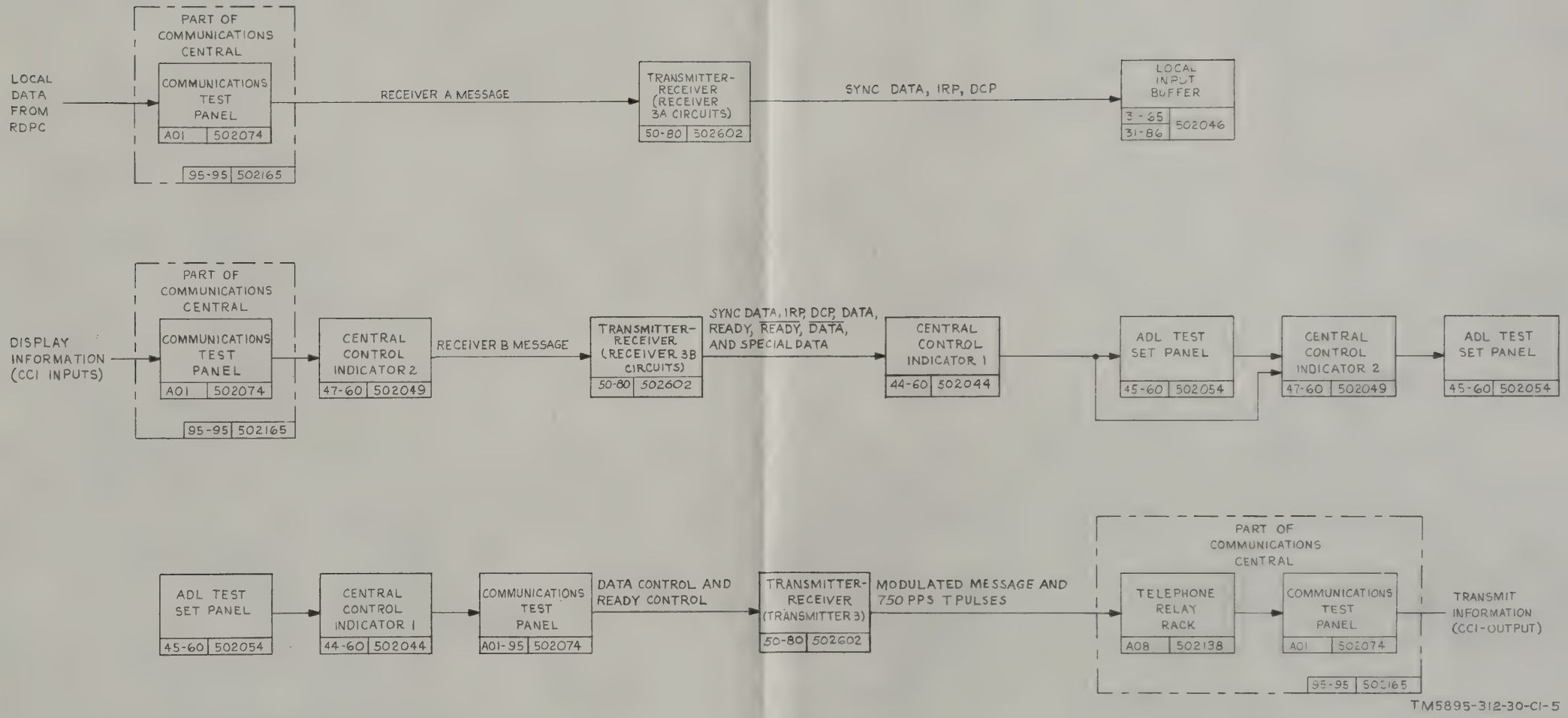
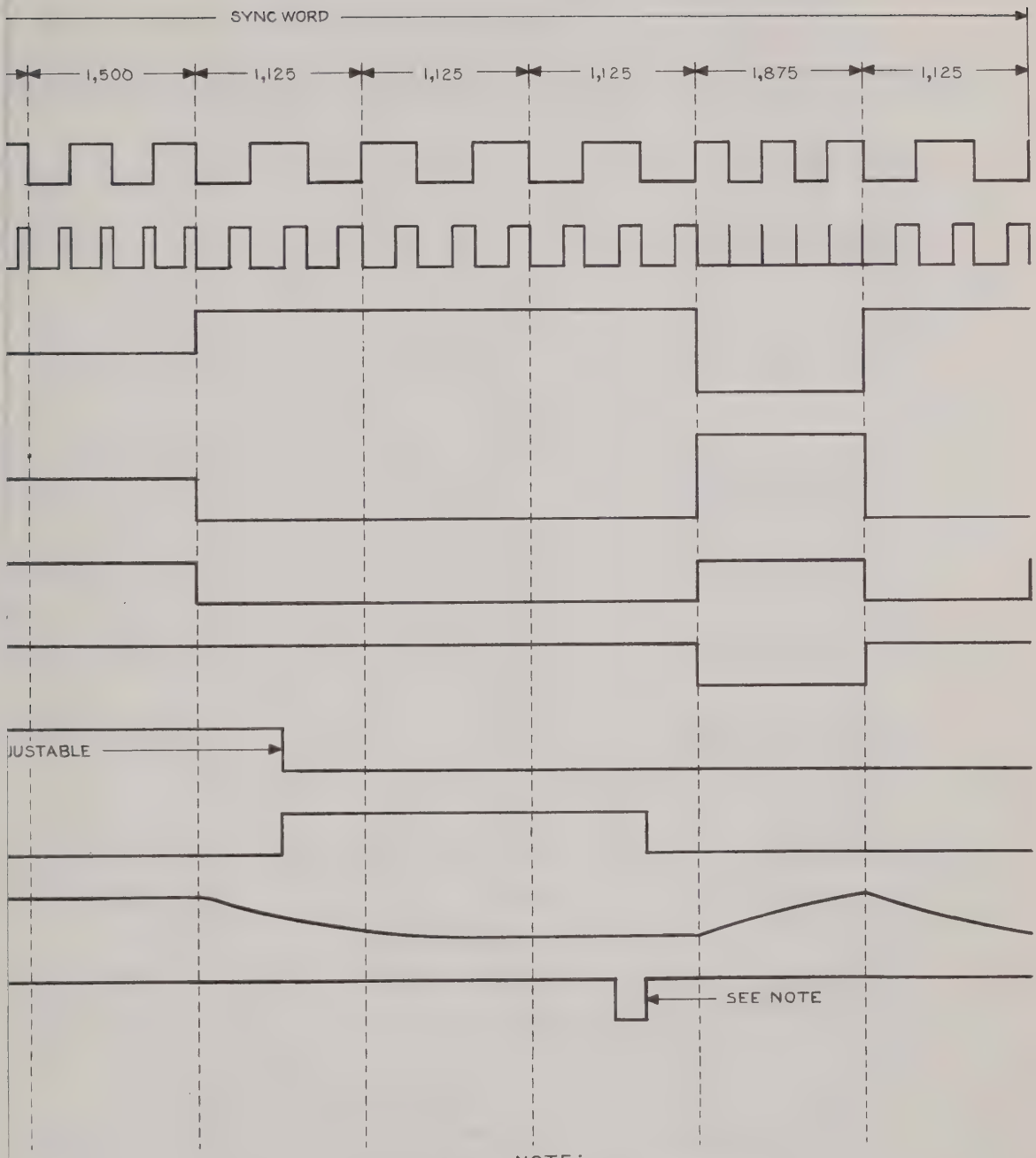


Figure 4. WMC transmitter-receiver 3, data flow, block diagram.



mote start detector timing diagram (part 1 of 2).

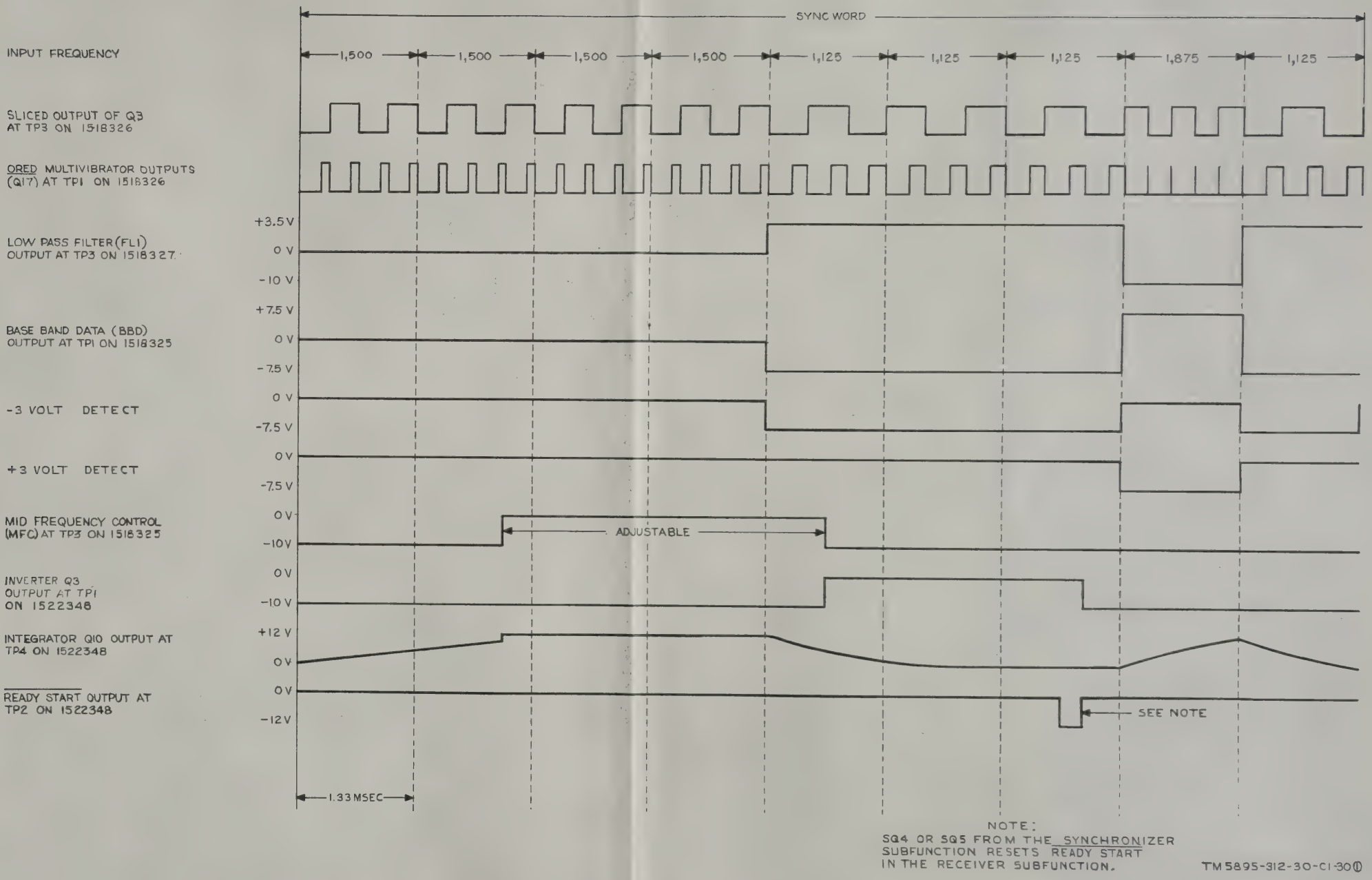
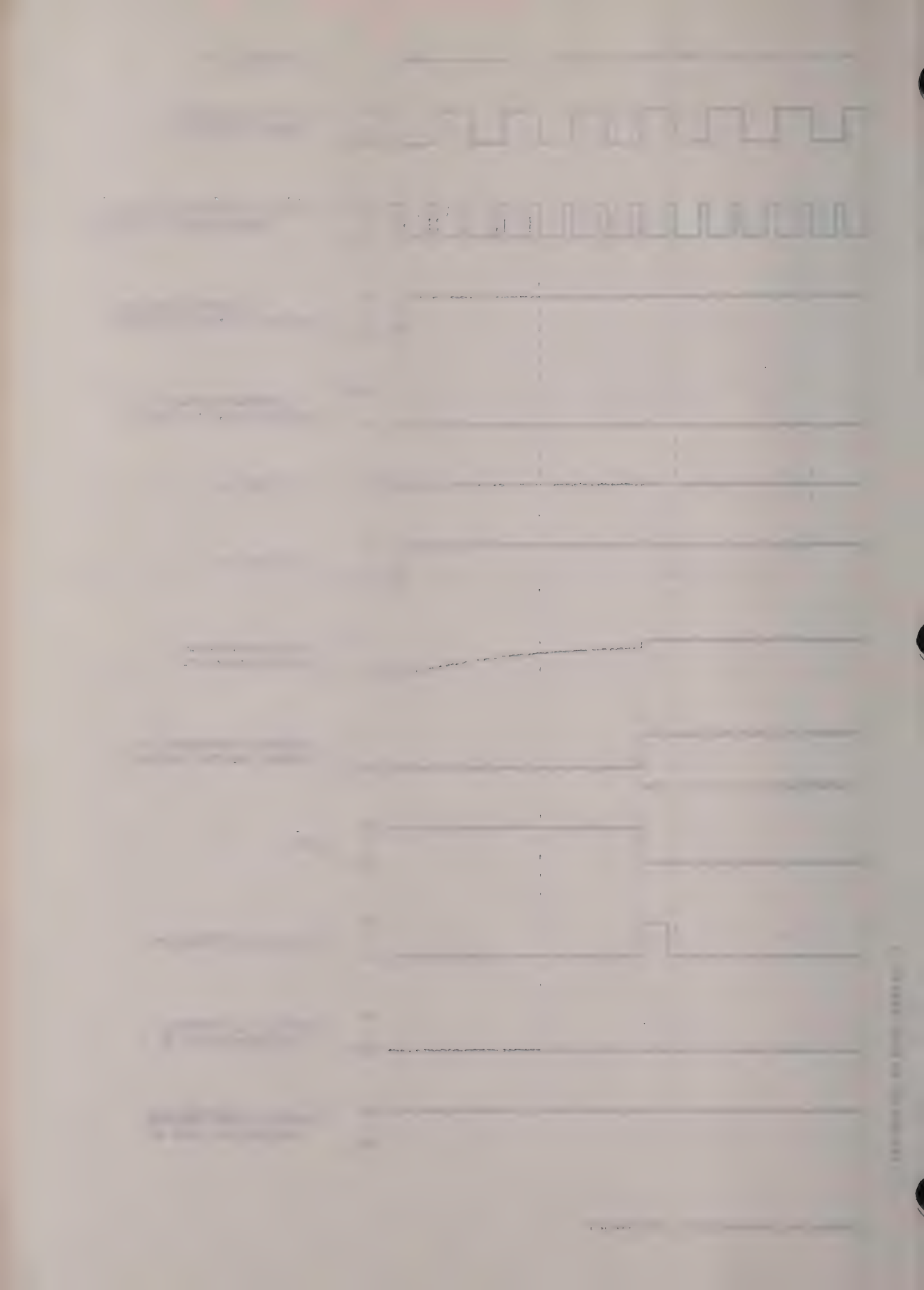


Figure 8①. FSM receiver and remote start detector timing diagram (part 1 of 2).

761-494 O - 65 Fols. Text No. 4



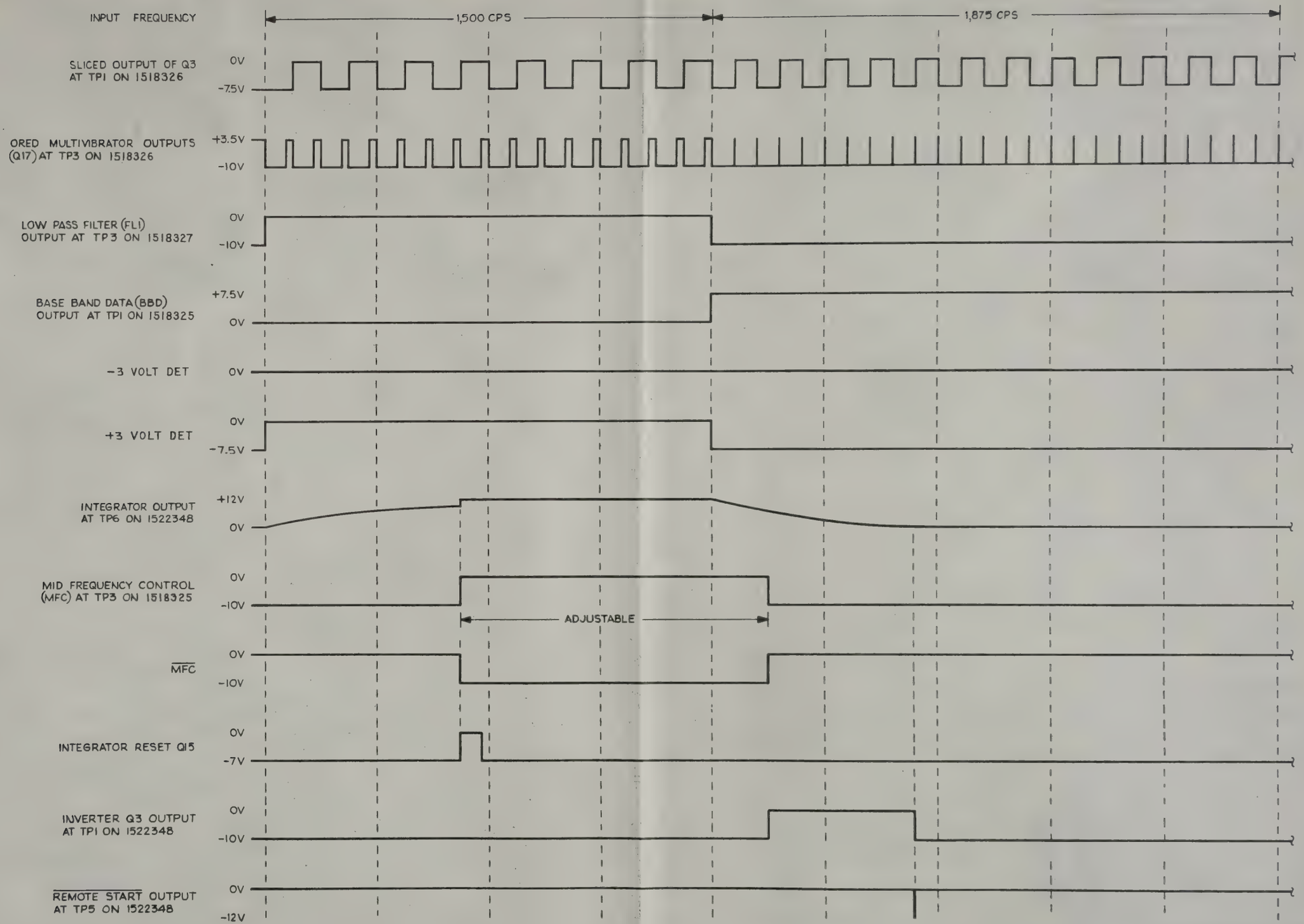
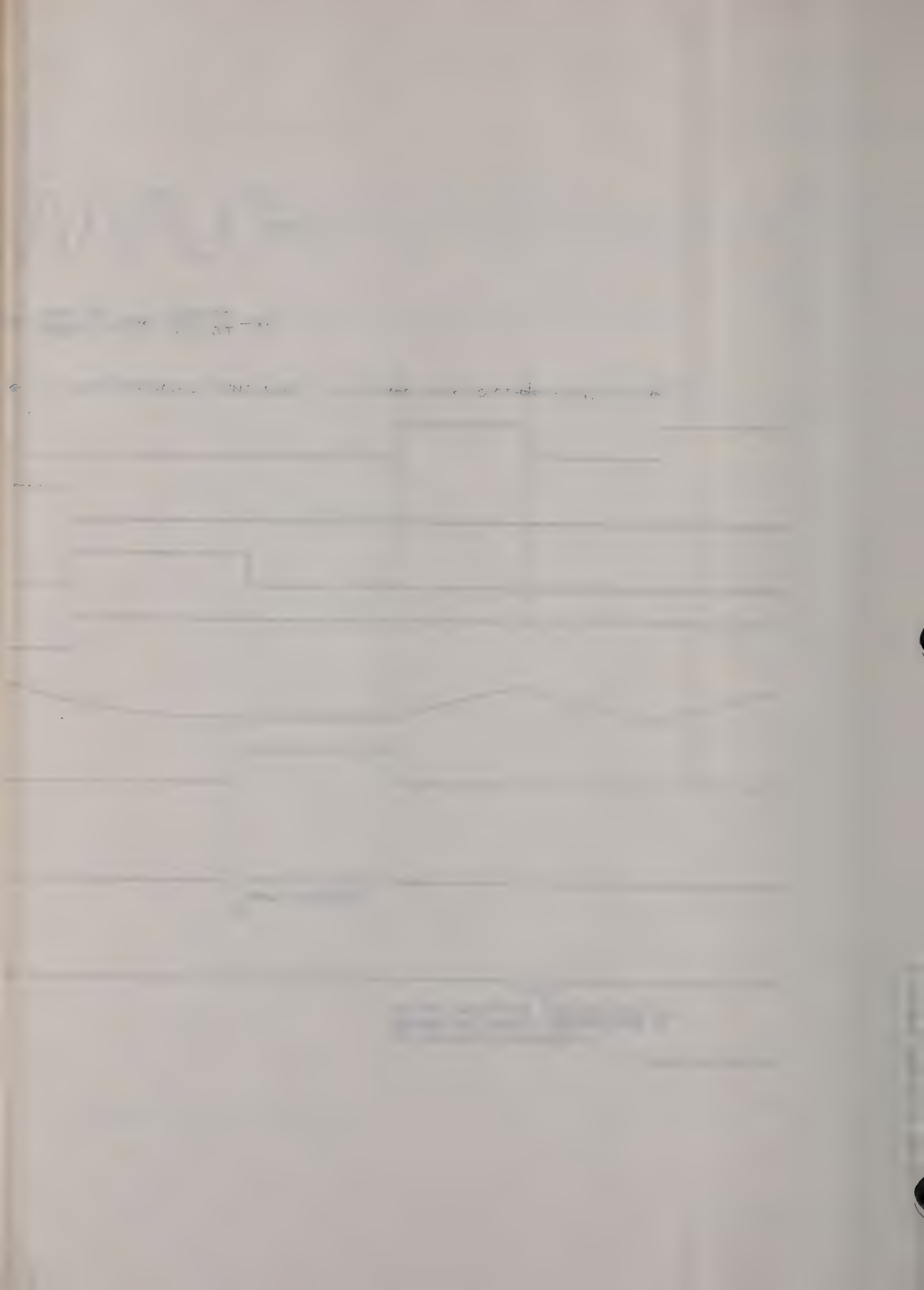
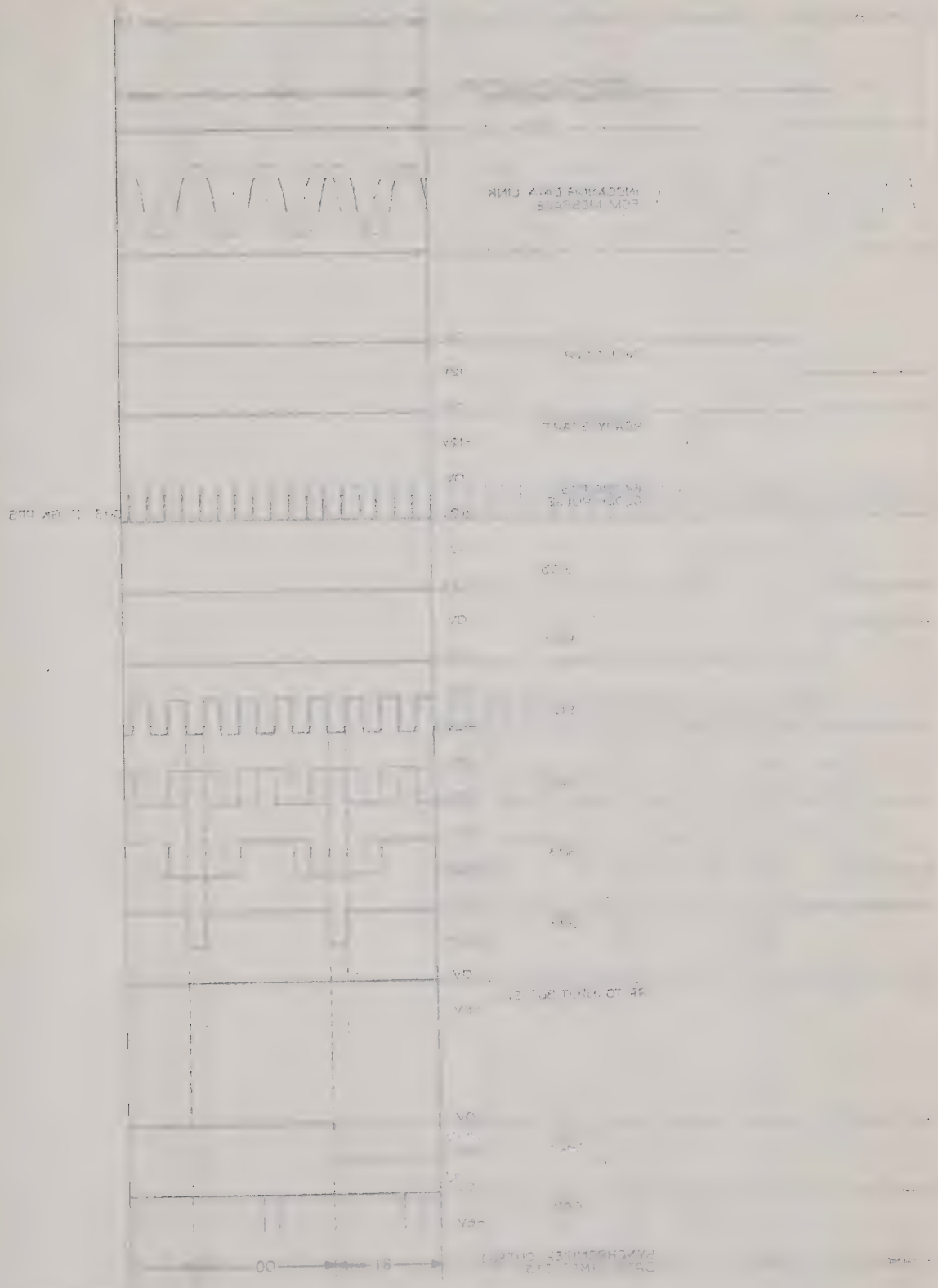


Figure 8②. FSM receiver and remote start detector timing diagram (part 2 of 2).





761-494 O - 65 Fols. Text No. 5

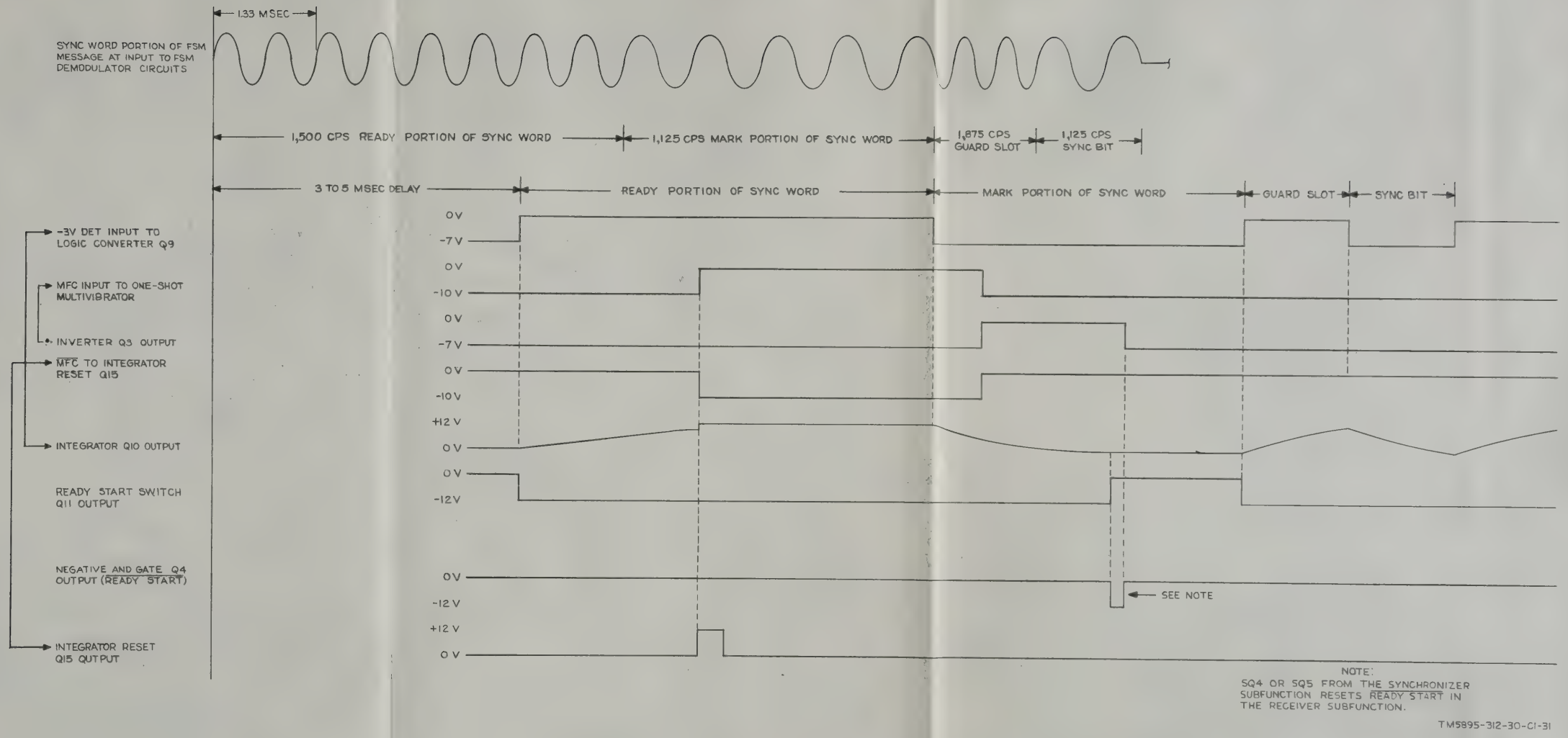


Figure 9. FSM ready start timing diagram.

761-494 O 65 - Fols. Text No. 6

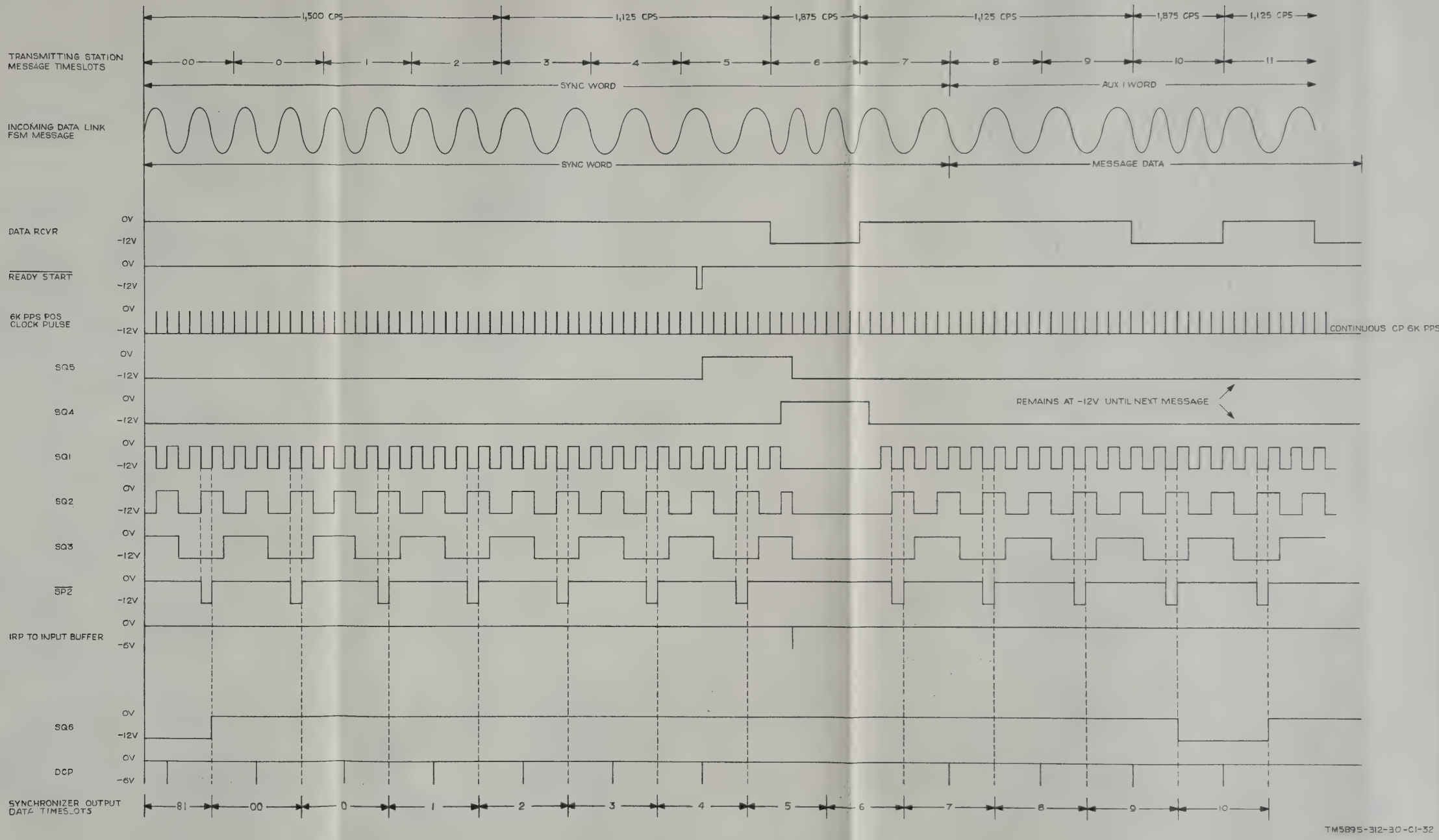


Figure 10. FSM synchronizer timing diagram.

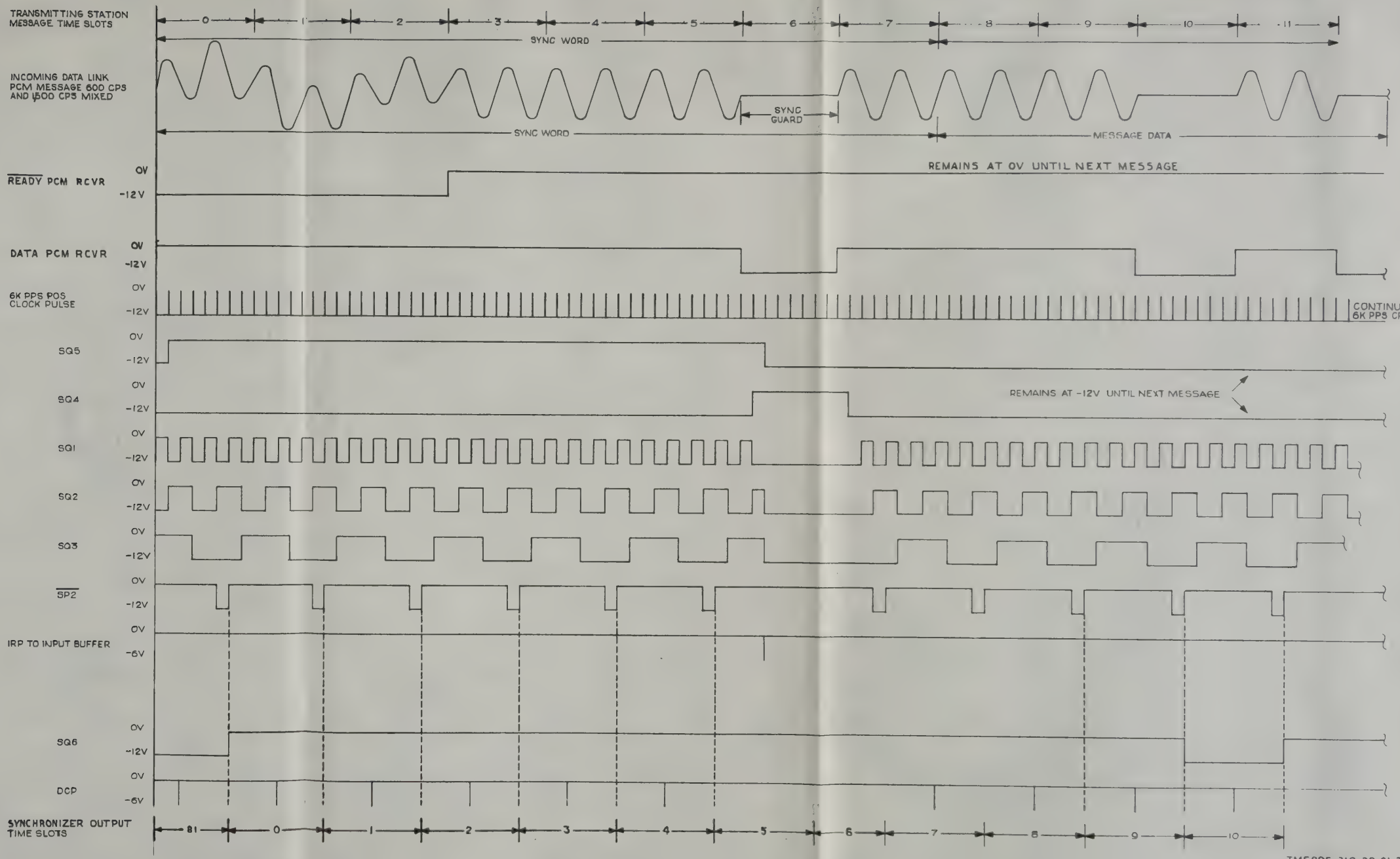
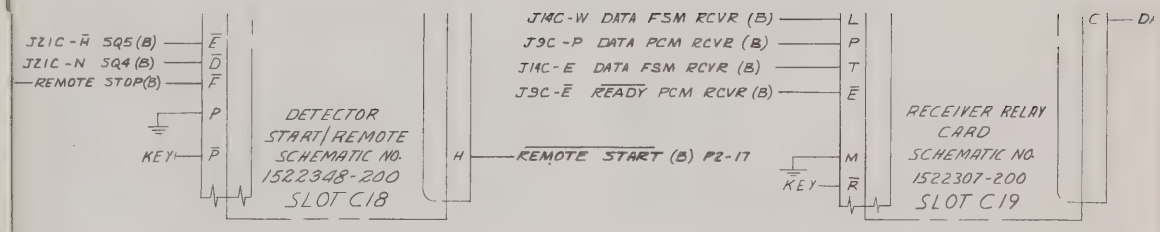


Figure 11. PCM synchronizer timing diagram.


J21C-H SQ5(B)
J21C-N SQ4(B)
REMOTE STOP(B)
KEY
DETECTOR START/REMOTE SCHEMATIC NO. 1522348-200 SLOT C18
REMOTE START (B) P2-17
J14C-W DATA FSM RCVR (B)
J9C-P DATA PCM RCVR (B)
J14C-E DATA FSM RCVR (B)
J9C-E READY PCM RCVR (B)
KEY
RECEIVER RELAY CARD SCHEMATIC NO. 1522307-200 SLOT C19

J10A
-50V — A
+50V — V
J12A-N — FSM/PCM MOD INPUT — N
J12A-B — ATTEN-INPUT — B
M
KEY — R
PART OF J10A
J12A
FSM MODULATED MESSAGE — J, K
FILTER OUTPUT — L
-27V REG — X
+18V REG — P
TEST — N, P
TP A-24 & 25
TP A-21
PCM MODULATED MESSAGE — J17A-V, J17A-Z
MODULATOR OUTPUT
SCHEMATIC NO. 1518484-200
SLOTS A10 — A11
DATA XMTR — F
-12V — A
J17A-V — V
J17A-Z — Z
+27V REG — M
-27V REG — X
J18A-W — FSM MODULATOR SIG — W
-26.5V — Y
AC RET — Z
J18A-W — 1500 CPS SQ WAVE — U
-6V — B
M
KEY — V
VARIABLE GRIN AMPLIFIER & TRANSMITTER RELAY CARD
SCHEMATIC NO. 1522312-200
SLOT A12
PART OF J12A
NOT USED — L
T PULSE COMM — C
ATTEN-INPUT — J10A-B — B
FSM/PCM MOD INPUT — J10A-N — N
PCM CONTROL — P2-16 — V
FSM CONTROL — P2-15 — T
1500 CPS DATA — J17A-D MODULATED — D
P2-9 MODULATED — N
P2-10 MESSAGE — P
MODE CONTROL — J13A-S — S
J13A
J9A-E — 6 KC SQ WAVE — E
DATA XMTR — F
READY XMTR — J
-12V — A
+12V — V
-6V — B
-28V — B
+1.5V — Z
J12A-S — MODE CONTROL — S
M
KEY — L
PART OF J13A
6 KC POS C.P — C
6 KC NEG C.P — A
DATA XMTR — J T A-H — H
READY XMTR — J T-K — K
750 PPS T PULSE — P2-E — X
6 KC & 750 PPS C.P. GENERATOR SCHEMATIC NO. 1518493-200
SLOT A13
J17A
+50V — V
+18V REG — P
+1.5V — Z
-27V REG — X
-6V — B
READY XMTR — J
J12A-D — 1500 CPS DATA MODULATED — D
M
KEY — S
J10B
TB2-B5 — SMOOTHED DATA (A) — J
TB2-B4 — SMOOTHED READY (A) — J
-6V — B
+28V — V
-28V — A
+1.5V — Z
-12V — B
M
KEY — D
PART OF J10B
P — DATA PCM RCVR (A) — J20B-P, P2-13
E — DATA PCM RCVR (A) — J20B-E, P2-2
READY PCM RCVR (A) — P2-3
READY PCM RCVR (A) — J20B-E, P2-4
NOT USED
SLICER
SCHEMATIC NO. 1518486-200
SLOT B-10
J11B
FSM RCVR (A) MESSAGE — J20B-C, J20B-D — C, D
-12V — A
+12V — V
P
KEY — H
PART OF J11B
U
FILTERED DATA (FSM)
KEY — L
DATA INPUT FILTER & FIRST LIMITER AMPLIFIER
SCHEMATIC NO. 1518324
SLOTS B11 — B12
J13B
-12V — A
+12V — V
P
U
KEY — L
PART OF J13B
Z
LIMITED DATA FSM
SECOND LIMITER AMPLIFIER & FREQUENCY DISCRIMINATOR
SCHEMATIC NO. 1518326
SLOTS B13 - B14
J15B
-12V — A
+12V — V
-28V — M
Z
P
KEY — V
PART OF J15B
J
BB
J10C
FSM RCVR (A) MESSAGE — J19C-C, J19C-D — C, D
-12V — A
+12V — V
P
KEY — H
PART OF J10C
U
FILTERED DATA (FSM)
DATA INPUT FILTER & FIRST LIMITER AMPLIFIER
SCHEMATIC NO. 1518324
SLOTS C10 — C11
J12C
U
-12V — A
+12V — V
P
KEY — L
PART OF J12C
Z
LIMITED DATA (FSM)
SECOND LIMITER AMPLIFIER & FREQUENCY DISCRIMINATOR
SCHEMATIC NO. 1518326
SLOTS C12 — C13
J14C
Z
-12V — A
+12V — V
-28V — M
P
KEY — V
PART OF J14C
J
W — DATA FSM RCVR (B)
E — DATA FSM RCVR (A)
H — NOT USED
DATA LOGIC AMPLIFIER
SCHEMATIC NO. 1518327
SLOTS C14 — C15

Figure 12

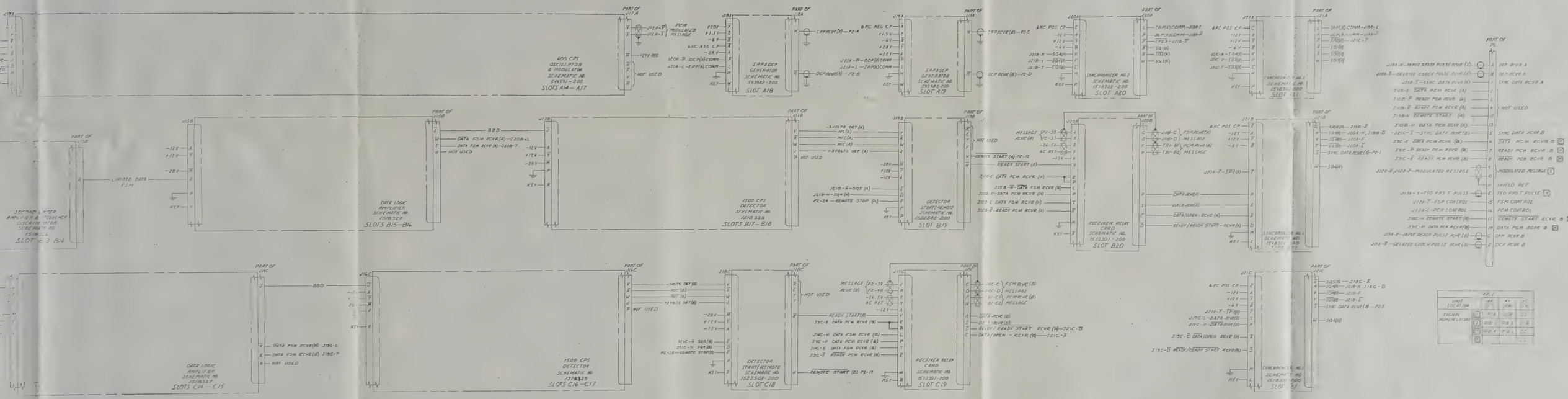


Figure 12①. Transmitter-receiver 502602, unit schematic diagram (part 1 of 2).

① DEPENDENT UPON UNIT LOCATION, PREFIX THE SIGNAL NOMENCLATURE IN ACCORDANCE WITH TABLE. THIS APPLIES TO THE WMC ONLY.

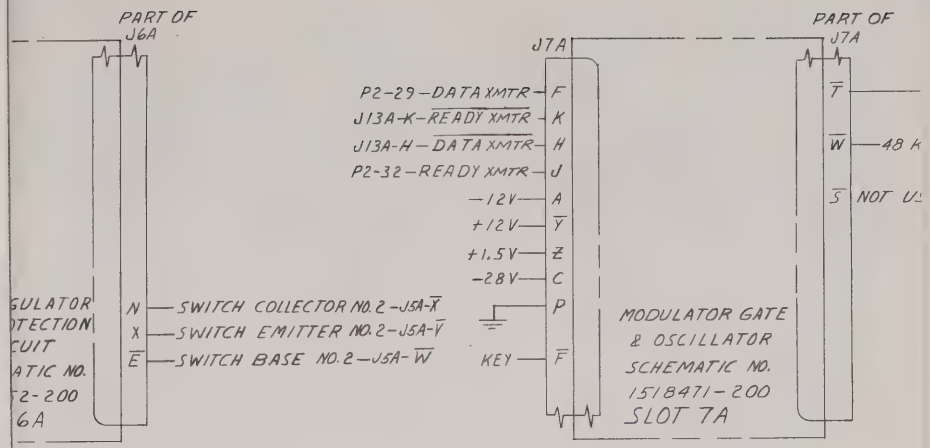
4. FOR UNIT REFERENCE DESIGNATION SEE GENERAL ARRANGEMENT DRAWING NUMBER 1510340(WMC) OR 1518398(ADPC).

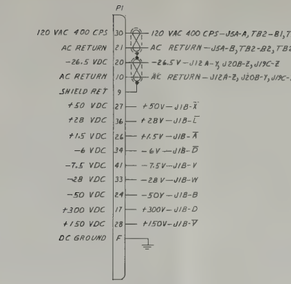
3. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.

2. FOR WIRING INFORMATION SEE DRAWING NUMBER 502602-300.

1. FOR ASSEMBLY SEE DRAWING NUMBER 1518376.

NOTES: UNLESS OTHERWISE SPECIFIED


PART OF
J6A
GULATOR
TECTION
CUIT
ATIC NO.
2-200
6A
N
X
E
SWITCH COLLECTOR NO. 2 - J5A-X
SWITCH EMITTER NO. 2 - J5A-Y
SWITCH BASE NO. 2 - J5A-W
J7A
P2-29 - DATA XMTR
J13A-K - READY XMTR
J13A-H - DATA XMTR
P2-32 - READY XMTR
-12V
+12V
+1.5V
-28V
KEY
F
K
H
J
A
Y
Z
C
P
F
MODULATOR GATE
& OSCILLATOR
SCHEMATIC NO.
1518471-200
SLOT 7A
PART OF
J7A
T
W
48 K
S
NOT U



P1 SPARES
1-8, 11-16, 18, 19, 22, 23, 25, 29, 31, 33, 35, 37-40, 42-48, A-E

P2 SPARES
18-23
26-28
33-36
41-48

LEVEL A TEST BLOCK

TP NO.	SIGNAL	TP NO.	SIGNAL	TP NO.	SIGNAL
1		15	DATA XMTR	29	+12 V
2		16	DATA XMTR	30	-12 V
3	T PULSE COMM	17	READY XMTR	31	DC GRD
4	1500 DATA MODULATED	18	READY XMTR	32	+27 V REG
5	750 PPS T PULSE	19	FSM MOD SIG	33	-27 V REG
6	MODULATED	20	1500 CPS SQ WAVE	34	+18 V REG
7	MESSAGE	21	FILTER OUTPUT	35	
8	TRP RCVR(A)	22	PCM MOD	36	
9	TRP RCVR(B)	23	MESSAGE	37	
10	DCP RCVR(A)	24	FSM MOD	38	
11	DCP RCVR(B)	25	MESSAGE	39	
12	6 MC POS CP	26		40	
13	6 MC NEG CP	27		41	
14		28		42	

LEVEL B TEST BLOCK

TP NO.	SIGNAL	TP NO.	SIGNAL	TP NO.	SIGNAL
1	SMOOTHED DATA (A)	15	REMOTE START (A)	29	+300V
2	SMOOTHED READY (A)	16	DATA FSM RCVR (A)	30	+150V
3	DATA PCM RCVR (A)	17	DATA FSM RCVR (A)	31	+50V
4	DATA PCM RCVR (A)	18	MFC (A)	32	+28V
5	READY PCM RCVR (A)	19	MFC (A)	33	+1.5V
6	READY PCM RCVR (A)	20	READY START (A)	34	DC GRD
7	SQ1 (A)	21	MESSAGE RCVR (A)	35	-6V
8	SQ2 (A)	22	MESSAGE RCVR (A)	36	-7.5V
9	SQ3 (A)	23	+3 VOLT DET (A)	37	-28V
10	SQ4 (A)	24	-3 VOLT DET (A)	38	-50V
11	SQ5 (A)	25	BRD (A)	39	
12	SQ6 (A)	26	SYNC DATA (A)	40	
13	SQ5 (A)	27		41	
14	SP2 (A)	28		42	

LEVEL C TEST BLOCK

TP NO.	SIGNAL	TP NO.	SIGNAL	TP NO.	SIGNAL
1	SMOOTHED DATA (B)	15	REMOTE START (B)	29	
2	SMOOTHED READY (B)	16	DATA FSM RCVR (B)	30	
3	DATA PCM RCVR (B)	17	DATA FSM RCVR (B)	31	
4	DATA PCM RCVR (B)	18	MFC (B)	32	
5	READY PCM RCVR (B)	19	MFC (B)	33	
6	READY PCM RCVR (B)	20	READY START (B)	34	
7	SQ1 (B)	21	MESSAGE RCVR (B)	35	
8	SQ2 (B)	22	MESSAGE RCVR (B)	36	
9	SQ3 (B)	23	+3 VOLT DET (B)	37	
10	SQ4 (B)	24	-3 VOLT DET (B)	38	
11	SQ5 (B)	25	BRD (B)	39	
12	SQ6 (B)	26	SYNC DATA (B)	40	
13	SQ5 (B)	27		41	
14	SP2 (B)	28		42	

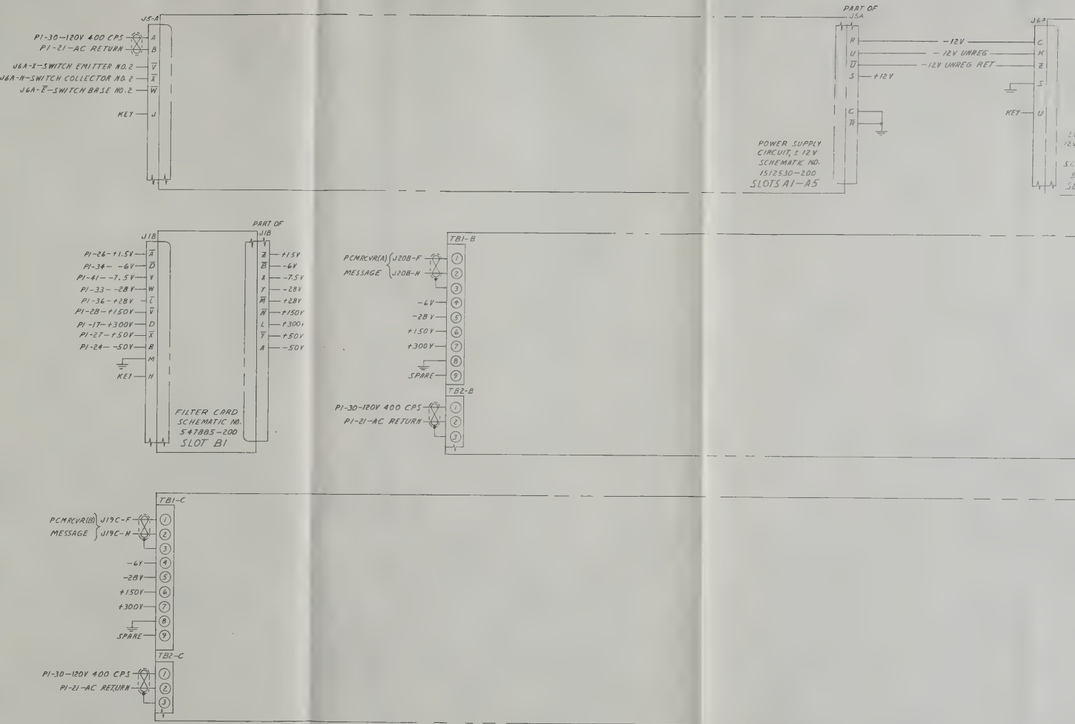


Figure 18©. Transmitter-receiver 502602, unit schematic diagram (part 2 of 2).

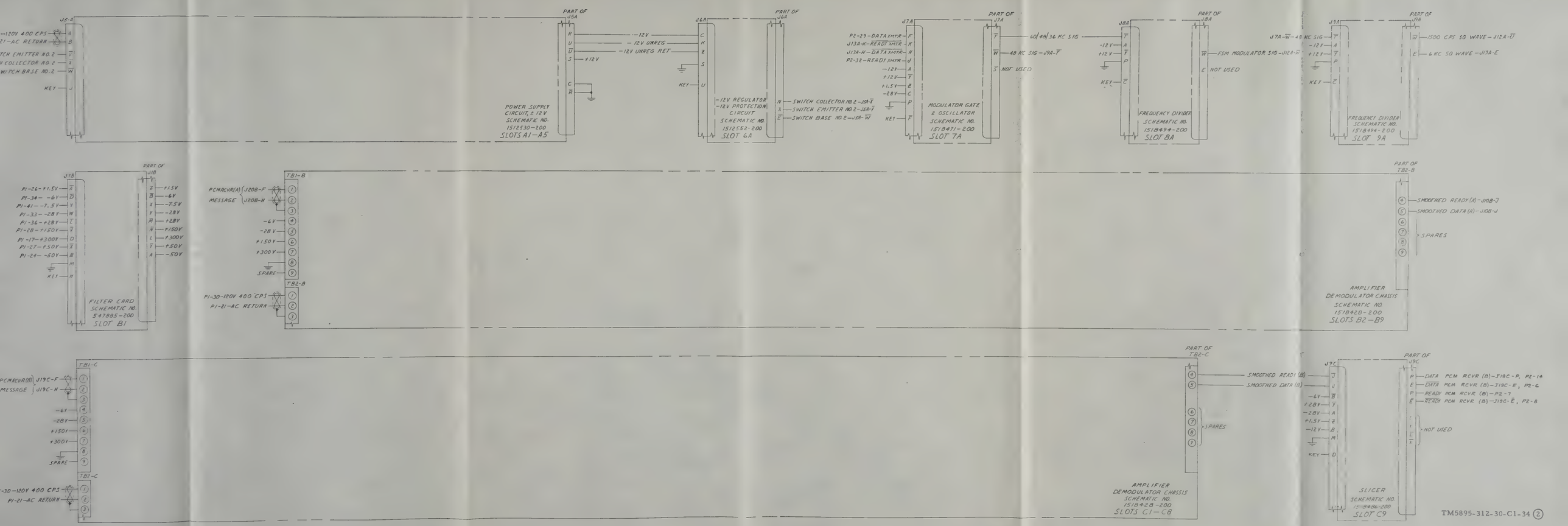
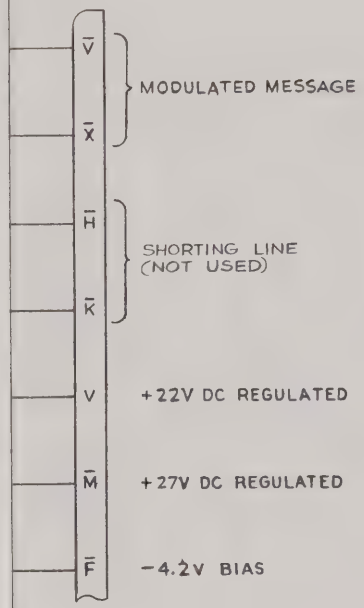


Figure 12②. Transmitter-receiver 502602, unit schematic diagram (part 2 of 2).

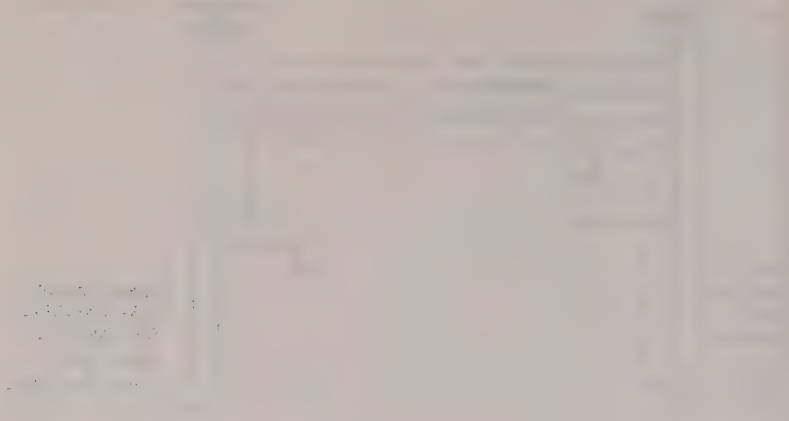
TM5895-312-30-C1-34 ②



NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF.
2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.

TM5895-312-30-14

761-494 O - 65 - Fols. Text No. 9



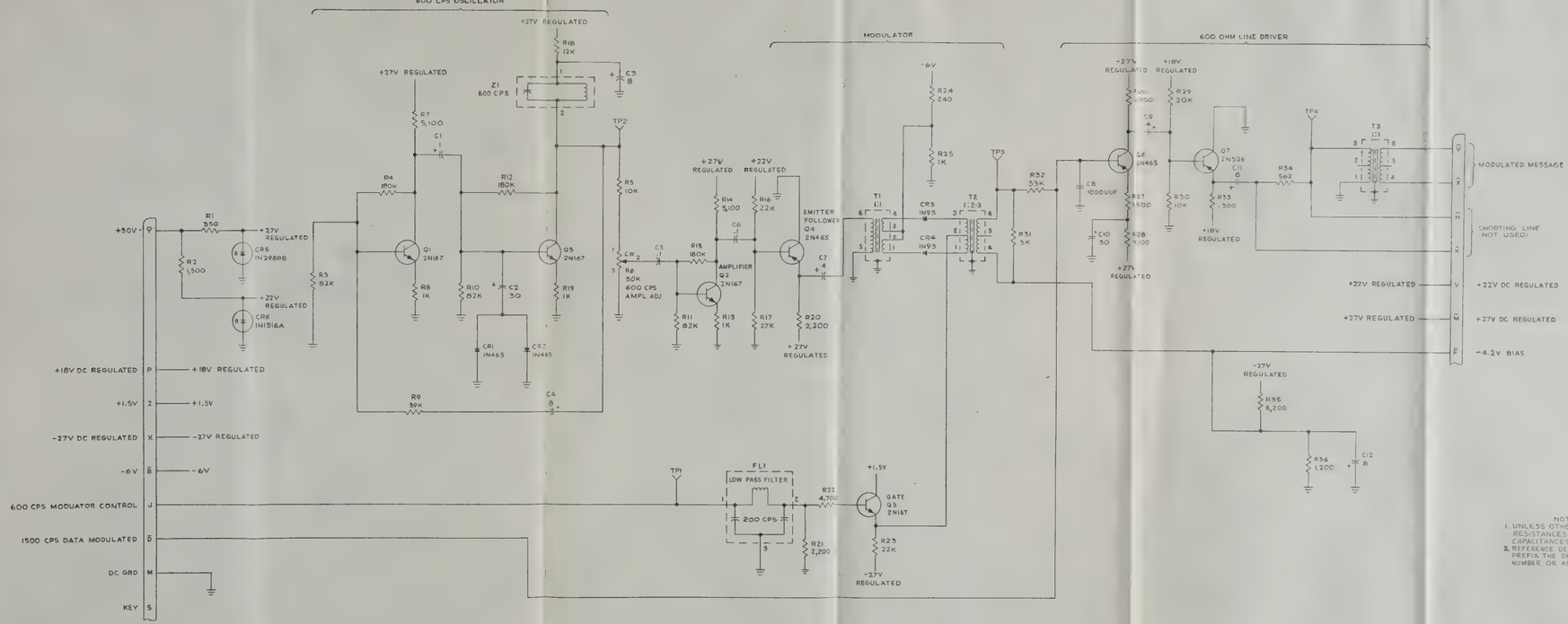
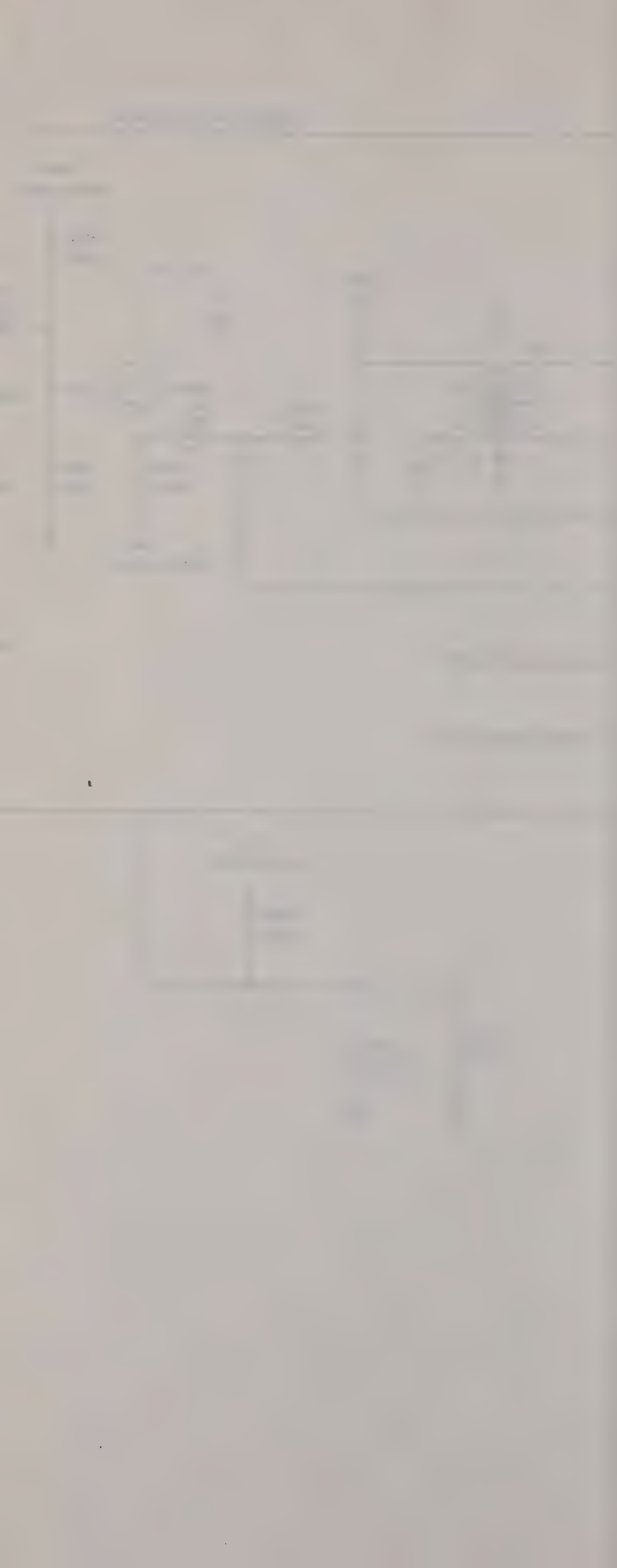
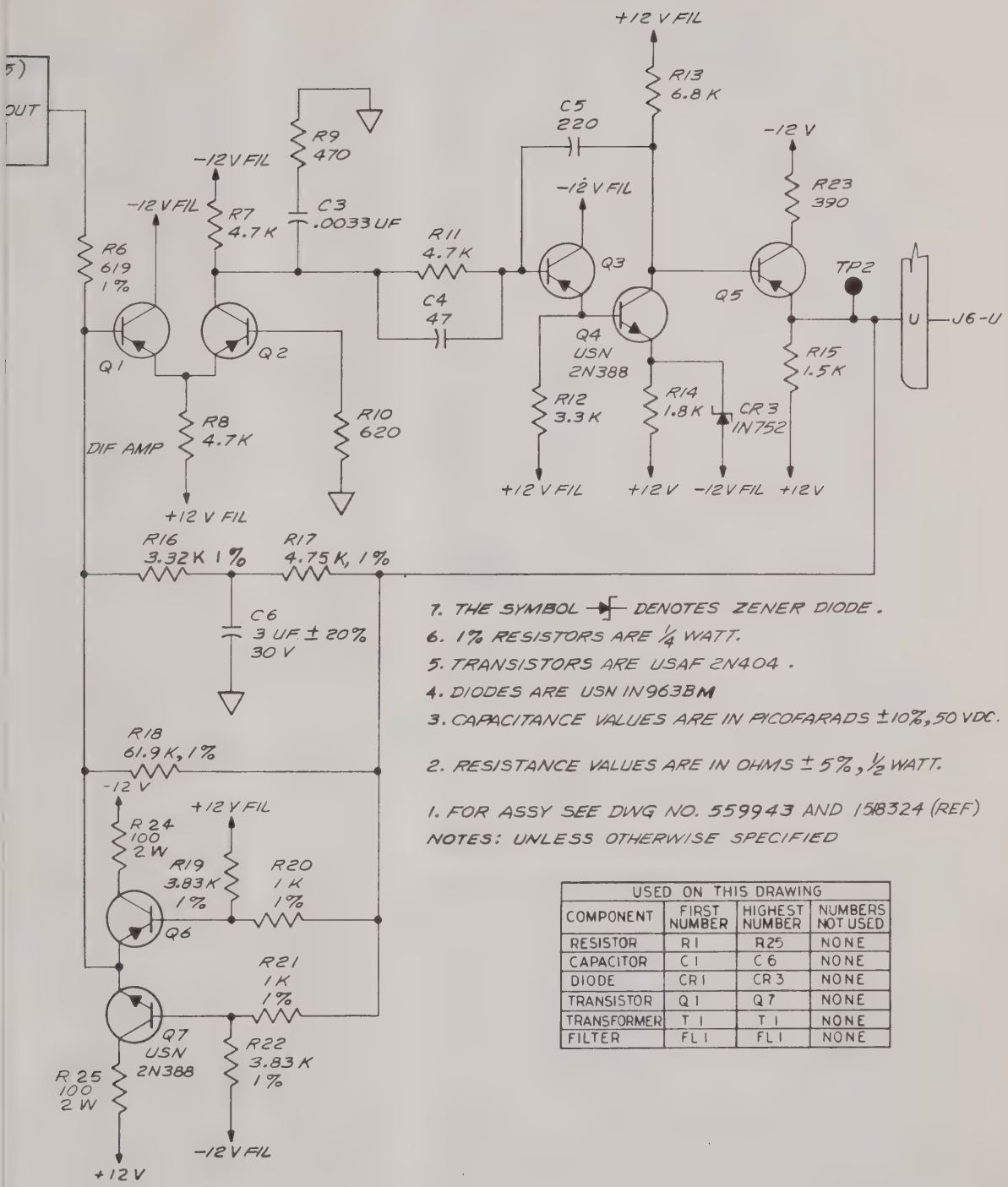


Figure 14. 600-cps oscillator and modulator 549591, schematic diagram.

NOTES
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN μF
2. REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX. THE DESIGNATIONS WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.

TM5895-312-30-14





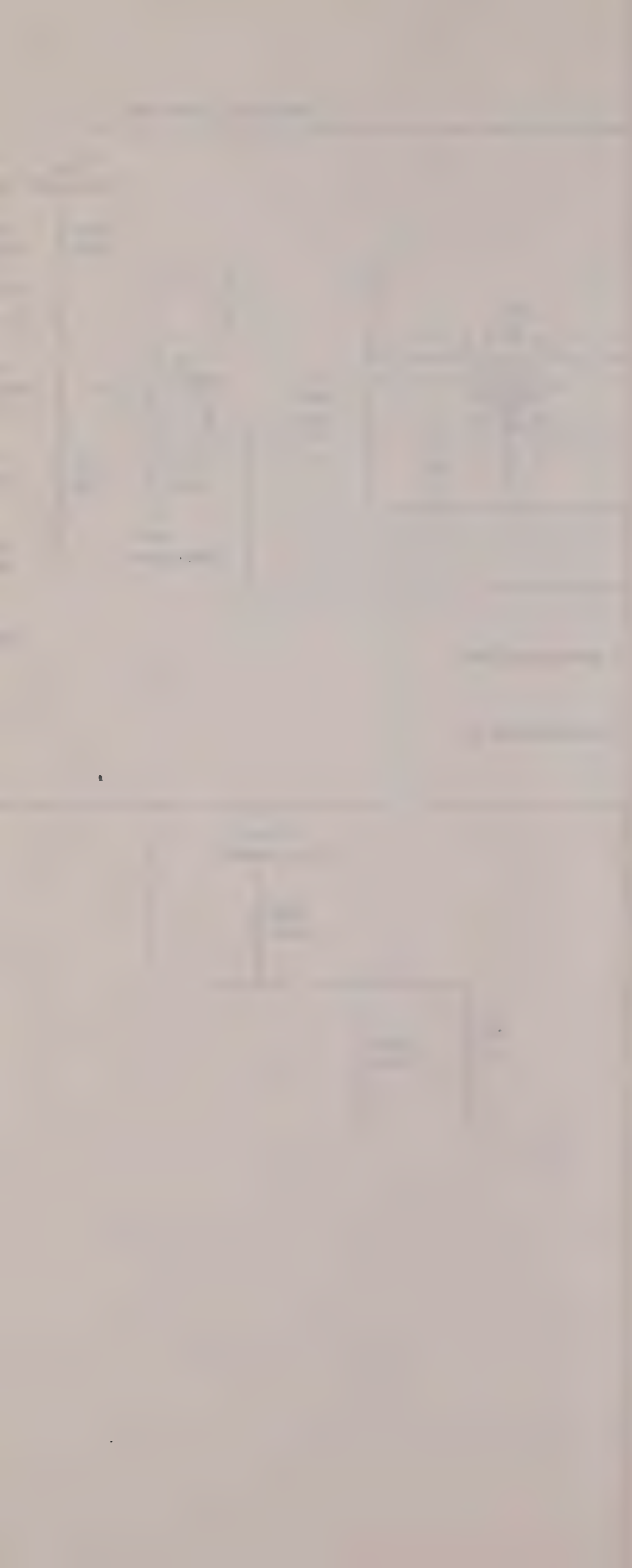
7. THE SYMBOL —▷|— DENOTES ZENER DIODE.
6. 1% RESISTORS ARE ¼ WATT.
5. TRANSISTORS ARE USAF 2N404.
4. DIODES ARE USN IN963BM
3. CAPACITANCE VALUES ARE IN PICOFARADS ±10%, 50 VDC.
2. RESISTANCE VALUES ARE IN OHMS ± 5%, ½ WATT.
1. FOR ASSY SEE DWG NO. 559943 AND 1518324 (REF)
NOTES: UNLESS OTHERWISE SPECIFIED

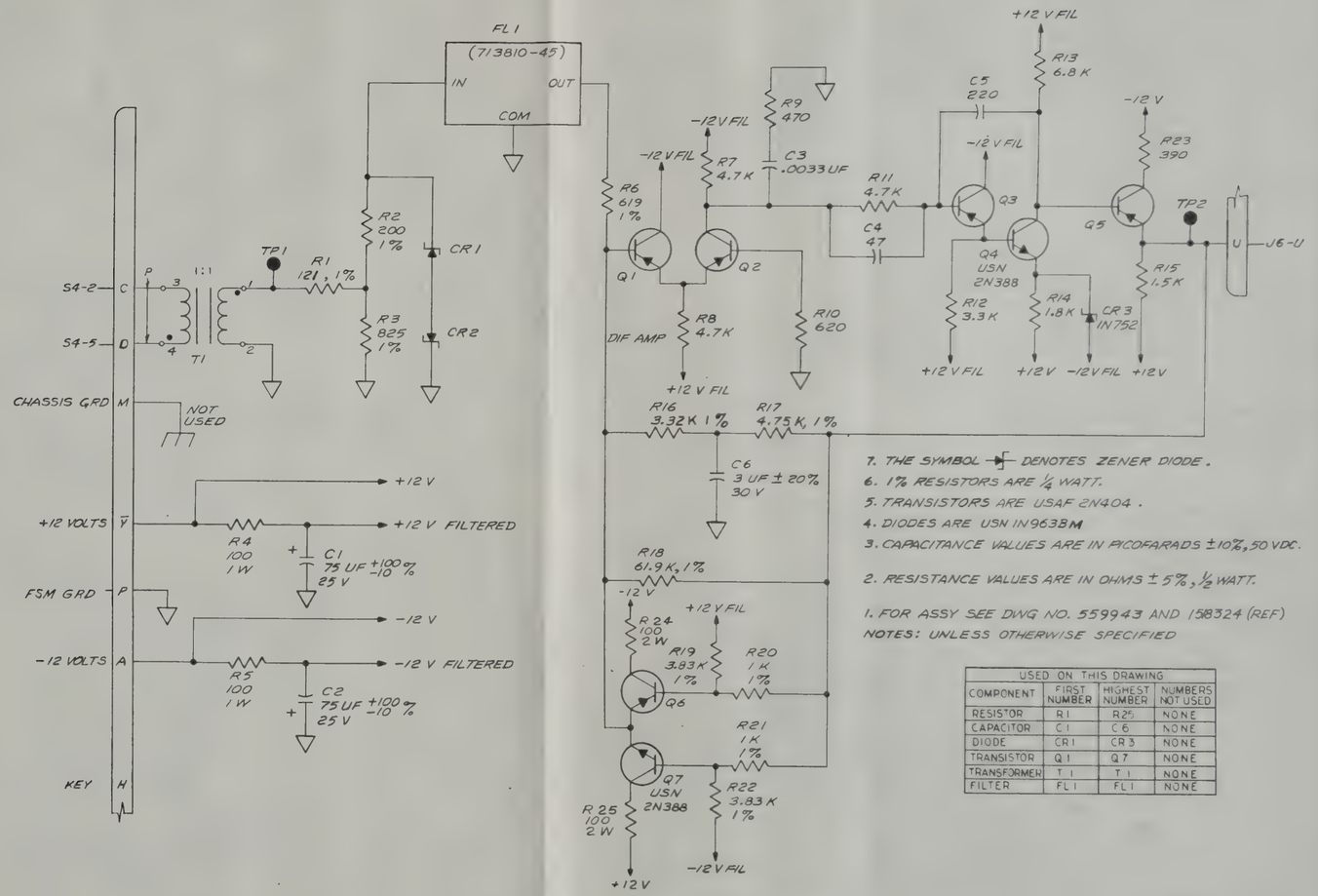
USED ON THIS DRAWING			
COMPONENT	FIRST NUMBER	HIGHEST NUMBER	NUMBERS NOT USED
RESISTOR	R1	R25	NONE
CAPACITOR	C1	C6	NONE
DIODE	CR1	CR3	NONE
TRANSISTOR	Q1	Q7	NONE
TRANSFORMER	T1	T1	NONE
FILTER	FL1	FL1	NONE

FEEDBACK LIMITERS

TM5895-312-30-35

ter and first limiter amplifier 1518324, schematic diagram.





7. THE SYMBOL → DENOTES ZENER DIODE.
6. 1% RESISTORS ARE ¼ WATT.
5. TRANSISTORS ARE USAF 2N404.
4. DIODES ARE USN IN963BM.
3. CAPACITANCE VALUES ARE IN PICOFARADS ±10%, 50 VDC.
2. RESISTANCE VALUES ARE IN OHMS ± 5%, ½ WATT.
1. FOR ASSY SEE DWG NO. 559943 AND 158324 (REF)
NOTES: UNLESS OTHERWISE SPECIFIED

USED ON THIS DRAWING			
COMPONENT	FIRST NUMBER	HIGHEST NUMBER	NUMBERS NOT USED
RESISTOR	R1	R25	NONE
CAPACITOR	C1	C6	NONE
DIODE	CR1	CR3	NONE
TRANSISTOR	Q1	Q7	NONE
TRANSFORMER	T1	T1	NONE
FILTER	FL1	FL1	NONE

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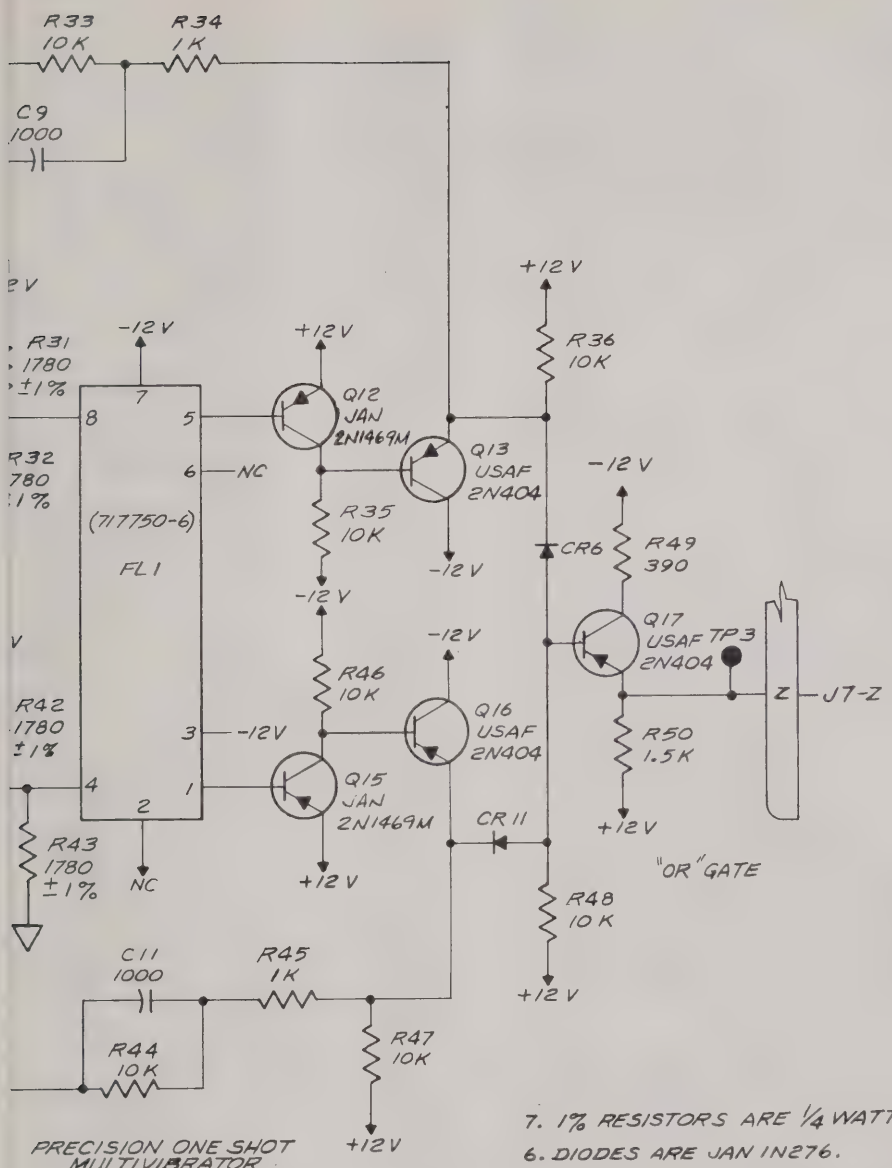
Figure 15. Data input filter and first limiter amplifier 1518324, schematic diagram.

781-494 O - 65 - Fols. Text No. 10



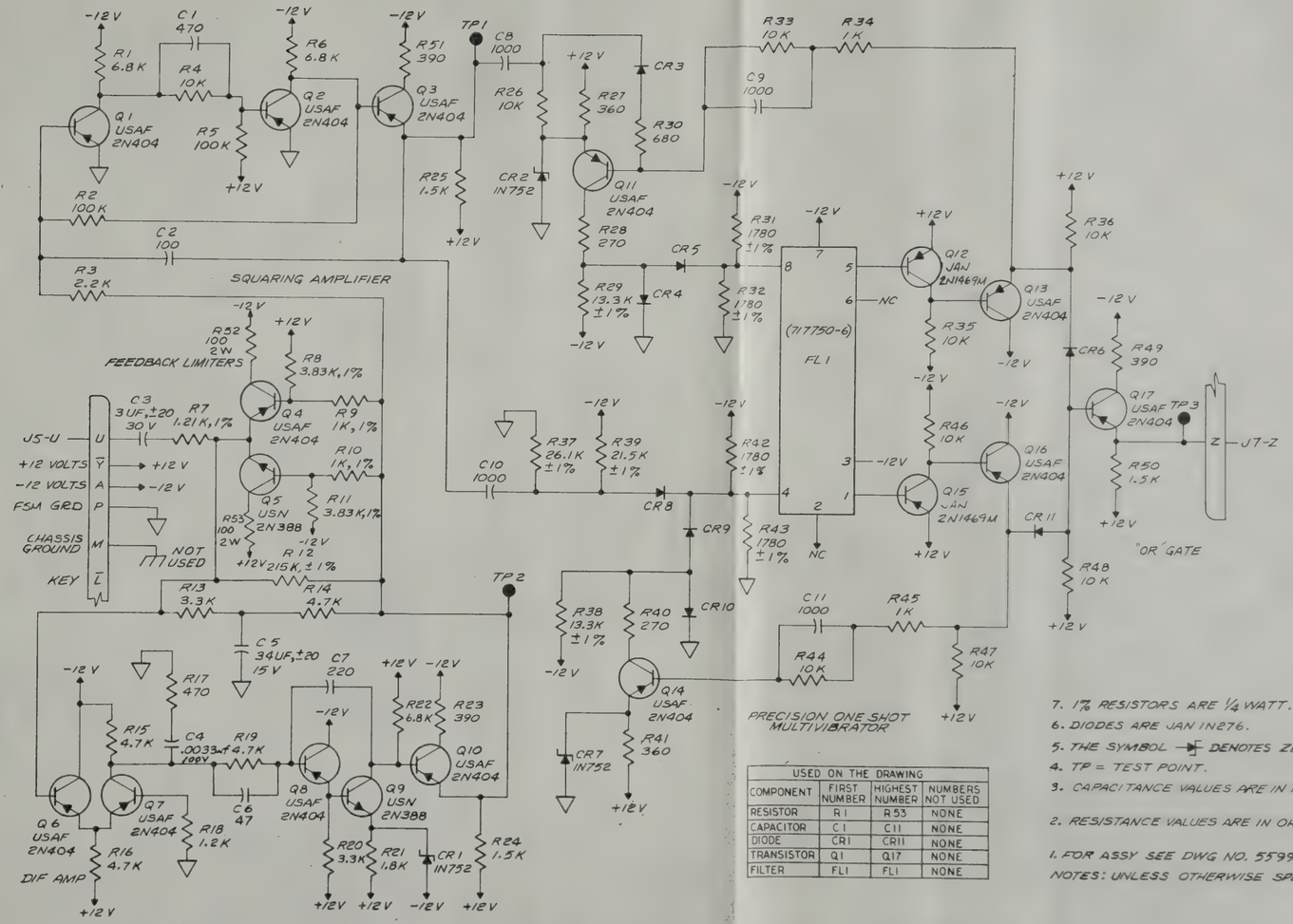
PRECISION ONE SHOT MULTIVIBRATOR

USED ON THE DRAWING			
COMPONENT	FIRST NUMBER	HIGHEST NUMBER	NUMBERS NOT USED
RESISTOR	R1	R53	NONE
CAPACITOR	C1	C11	NONE
DIODE	CR1	CR11	NONE
TRANSISTOR	Q1	Q17	NONE
FILTER	FL1	FL1	NONE

7. 1% RESISTORS ARE 1/4 WATT.
6. DIODES ARE JAN 1N276.
5. THE SYMBOL —▶|— DENOTES ZENER DIODE.
4. TP = TEST POINT.
3. CAPACITANCE VALUES ARE IN PICOFARAD ±5%, 50 V.
2. RESISTANCE VALUES ARE IN OHMS ±5%, 1/2 WATT.
1. FOR ASSY SEE DWG NO. 559948 AND 1518326 (REF)
NOTES: UNLESS OTHERWISE SPECIFIED

TM5895-312-30-36

...ncy discriminator 1518326, schematic diagram.



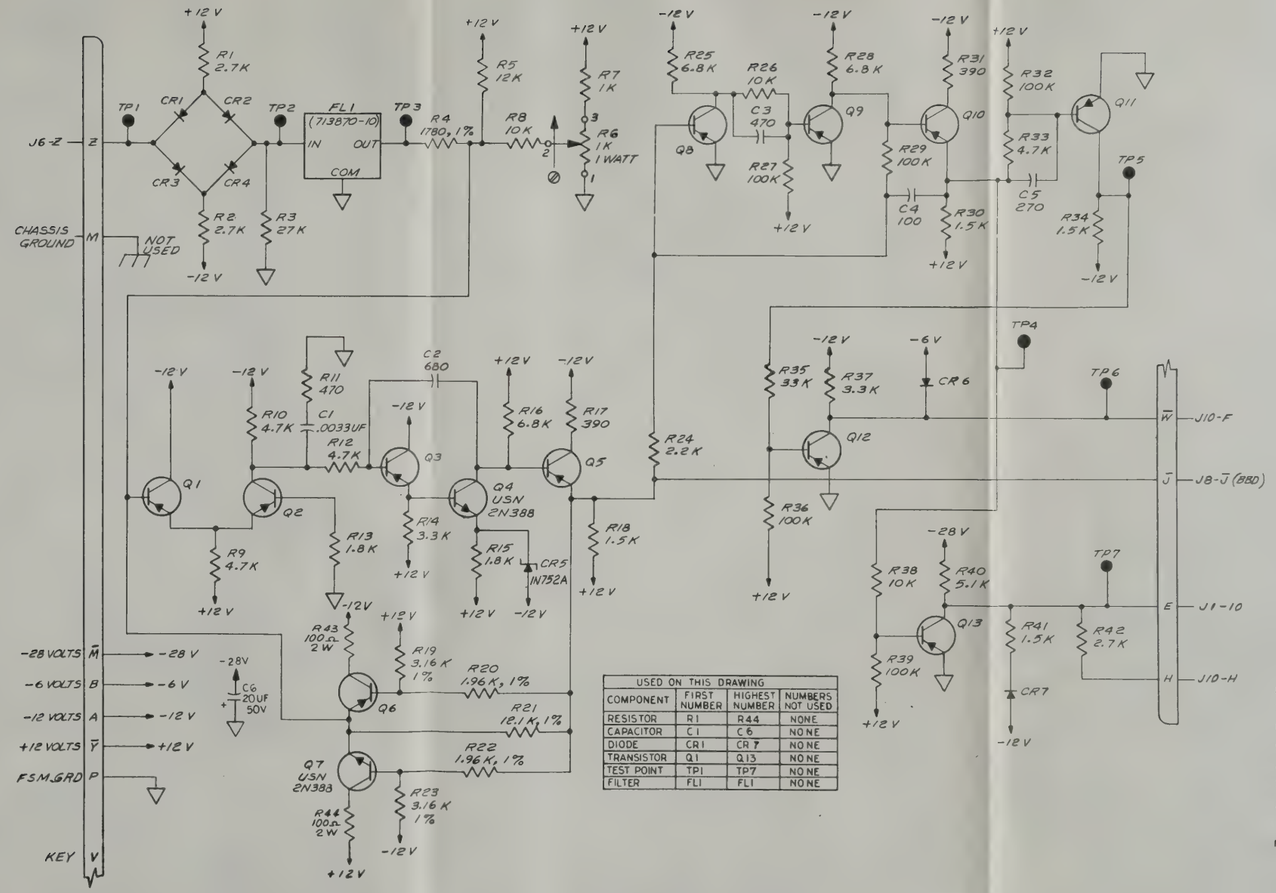
USED ON THE DRAWING			
COMPONENT	FIRST NUMBER	HIGHEST NUMBER	NUMBERS NOT USED
RESISTOR	R1	R53	NONE
CAPACITOR	C1	C11	NONE
DIODE	CR1	CR11	NONE
TRANSISTOR	Q1	Q17	NONE
FILTER	FL1	FL1	NONE

7. 1% RESISTORS ARE 1/4 WATT.
6. DIODES ARE JAN 1N276.
5. THE SYMBOL —▷|— DENOTES ZENER DIODE.
4. TP = TEST POINT.
3. CAPACITANCE VALUES ARE IN PICOFARAD ±5%, 50 V.
2. RESISTANCE VALUES ARE IN OHMS ±5%, 1/2 WATT.
1. FOR ASSY SEE DWG NO. 559948 AND 1518326 (REF)

NOTES: UNLESS OTHERWISE SPECIFIED

TM5895-312-30-36

Figure 16. Second limiter amplifier and frequency discriminator 1518326, schematic diagram.



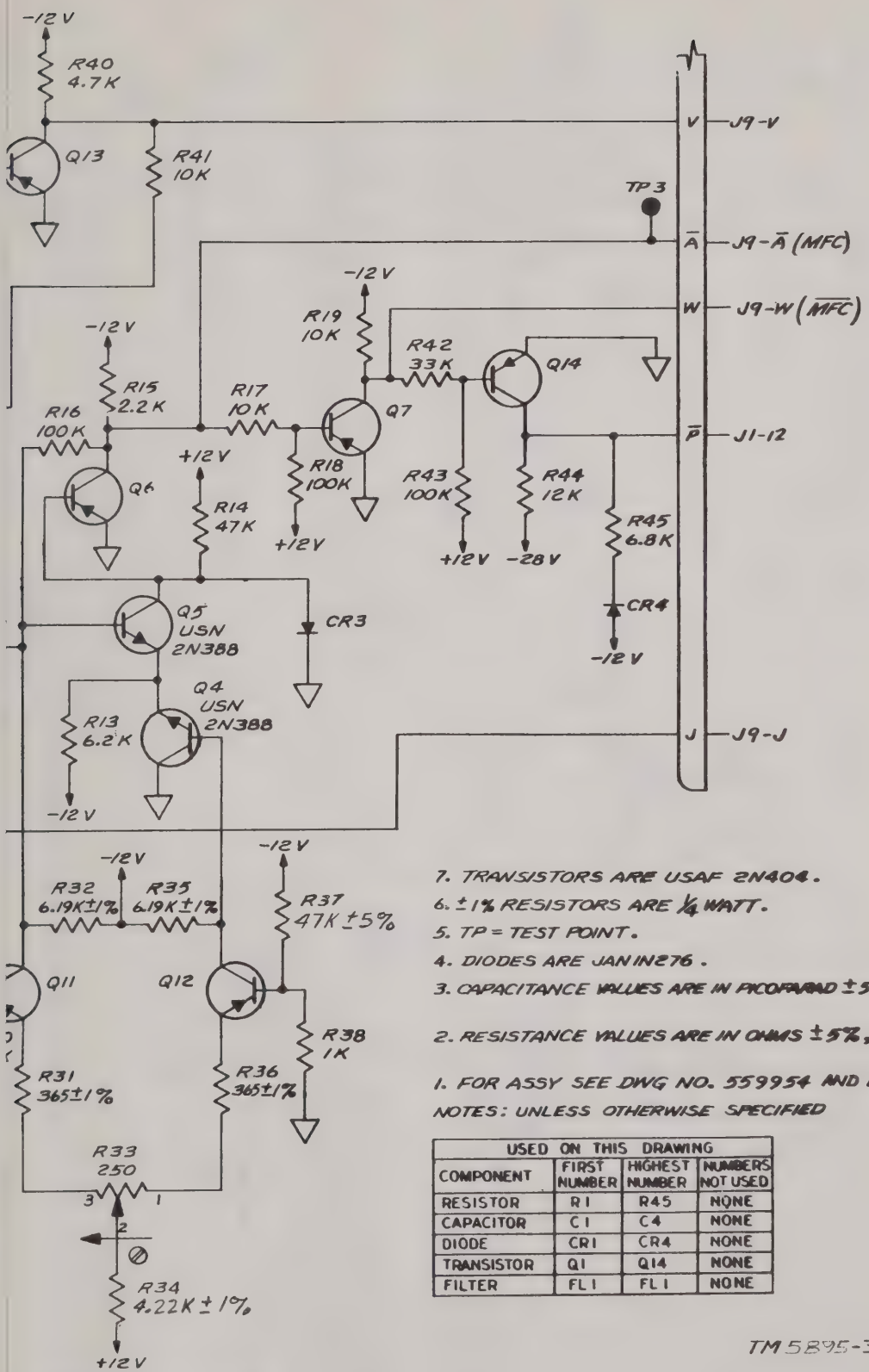
USED ON THIS DRAWING			
COMPONENT	FIRST NUMBER	HIGHEST NUMBER	NUMBERS NOT USED
RESISTOR	R1	R44	NONE
CAPACITOR	C1	C6	NONE
DIODE	CR1	CR7	NONE
TRANSISTOR	Q1	Q13	NONE
TEST POINT	TP1	TP7	NONE
FILTER	FL1	FL1	NONE

8 TP = TEST POINT
7 1% RESISTORS ARE 1/4 WATT
6 THE SYMBOL —▷|— DENOTES ZENER DIODE
5 TRANSISTORS ARE USAF 2N404
4 DIODES ARE JAN 1N276
3 CAPACITANCE VALUES ARE IN PICOFARADS ±10%, 50 VOLTS
2 RESISTANCE VALUES ARE IN OHMS ± 5%, 1/2 WATT
1 FOR ASSY SEE DWG NO. 559951 AND 1518327 (REF)
NOTES: UNLESS OTHERWISE SPECIFIED

TM5895-312-30-37

Figure 17. Data logic amplifier 1518327, schematic diagram.

761-494 O - 65 - Pols. Text No. 13

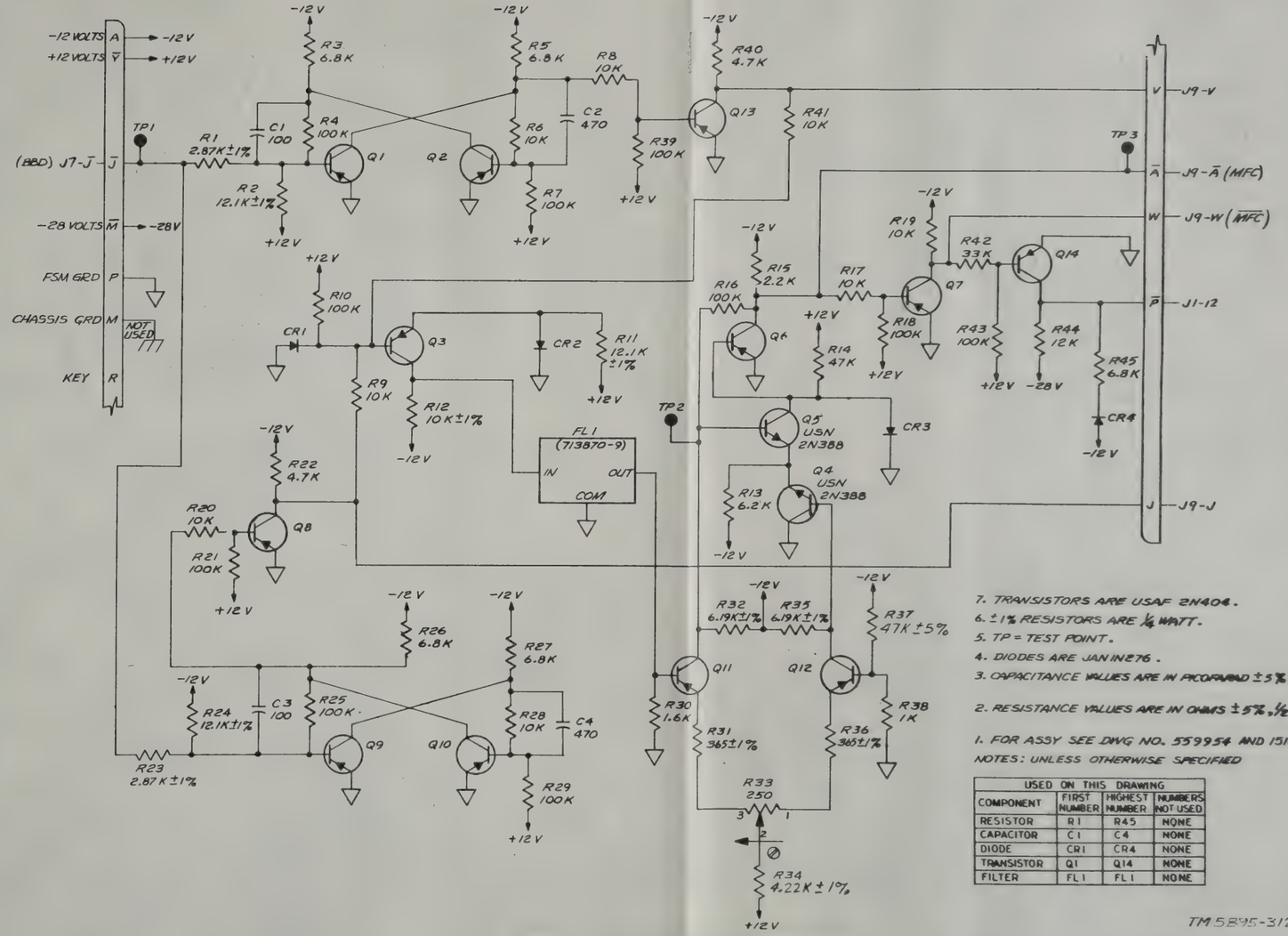


7. TRANSISTORS ARE USAF 2N404.
6. ±1% RESISTORS ARE ¼ WATT.
5. TP = TEST POINT.
4. DIODES ARE JAN1N276.
3. CAPACITANCE VALUES ARE IN PICOFARAD ±5%, 50 VOLTS.
2. RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT.
1. FOR ASSY SEE DWG NO. 559954 AND 1518325 (REF)
NOTES: UNLESS OTHERWISE SPECIFIED

USED ON THIS DRAWING			
COMPONENT	FIRST NUMBER	HIGHEST NUMBER	NUMBERS NOT USED
RESISTOR	R1	R45	NONE
CAPACITOR	C1	C4	NONE
DIODE	CR1	CR4	NONE
TRANSISTOR	Q1	Q14	NONE
FILTER	FL1	FL1	NONE

TM 5895-312-30-31-38

r 1518325, schematic diagram.



7. TRANSISTORS ARE USAF 2N404.
6. ±1% RESISTORS ARE ¼ WATT.
5. TP = TEST POINT.
4. DIODES ARE JAN IN276.
3. CAPACITANCE VALUES ARE IN PICOFARAD ±5%, 50 VOLTS.
2. RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT.
1. FOR ASSY SEE DWG NO. 559954 AND 1518325 (REF)
NOTES: UNLESS OTHERWISE SPECIFIED

USED ON THIS DRAWING			
COMPONENT	FIRST NUMBER	HIGHEST NUMBER	NUMBERS NOT USED
RESISTOR	R1	R45	NONE
CAPACITOR	C1	C4	NONE
DIODE	CR1	CR4	NONE
TRANSISTOR	Q1	Q14	NONE
FILTER	FL1	FL1	NONE

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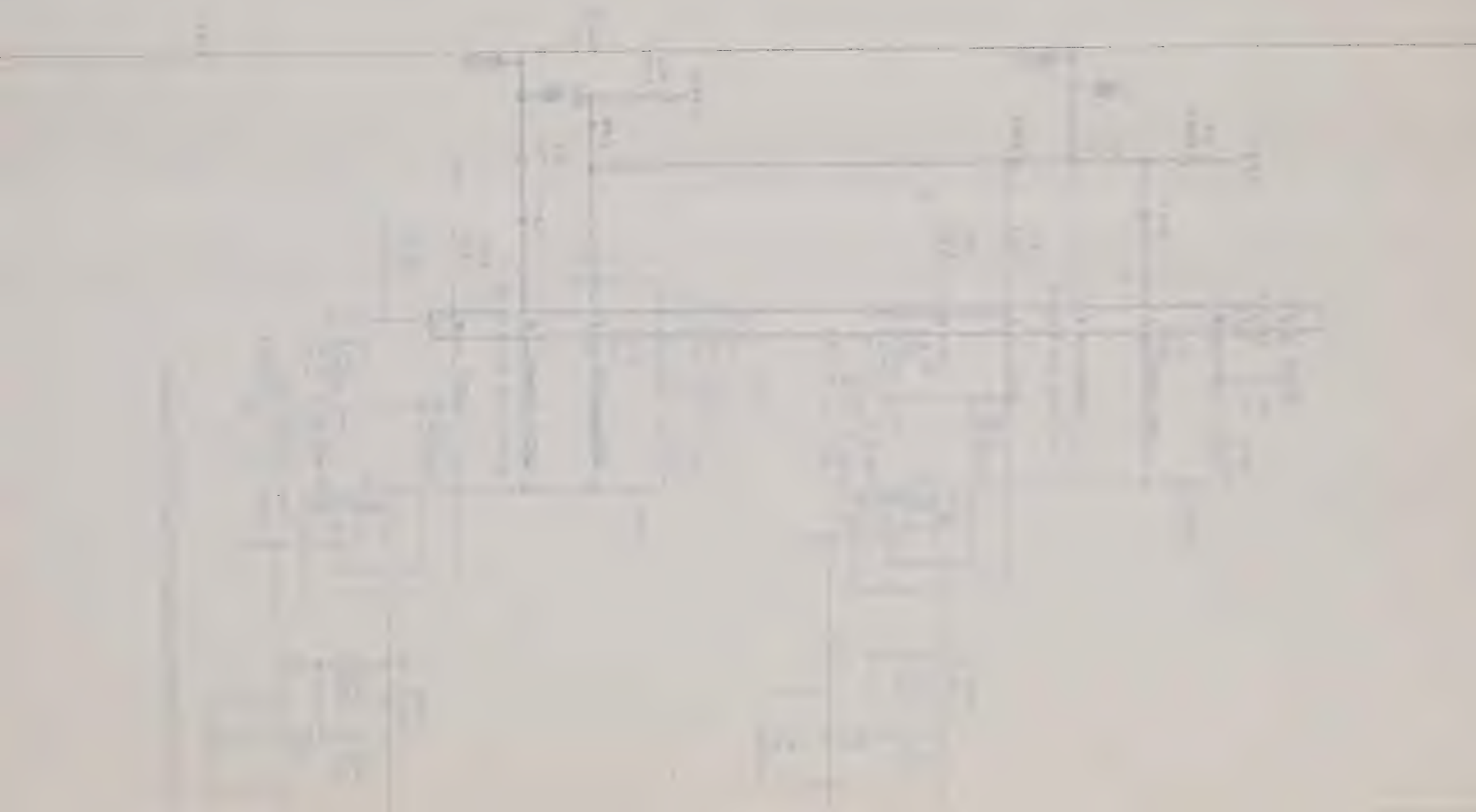
Figure 18. 1,500-cps detector 1518325, schematic diagram.



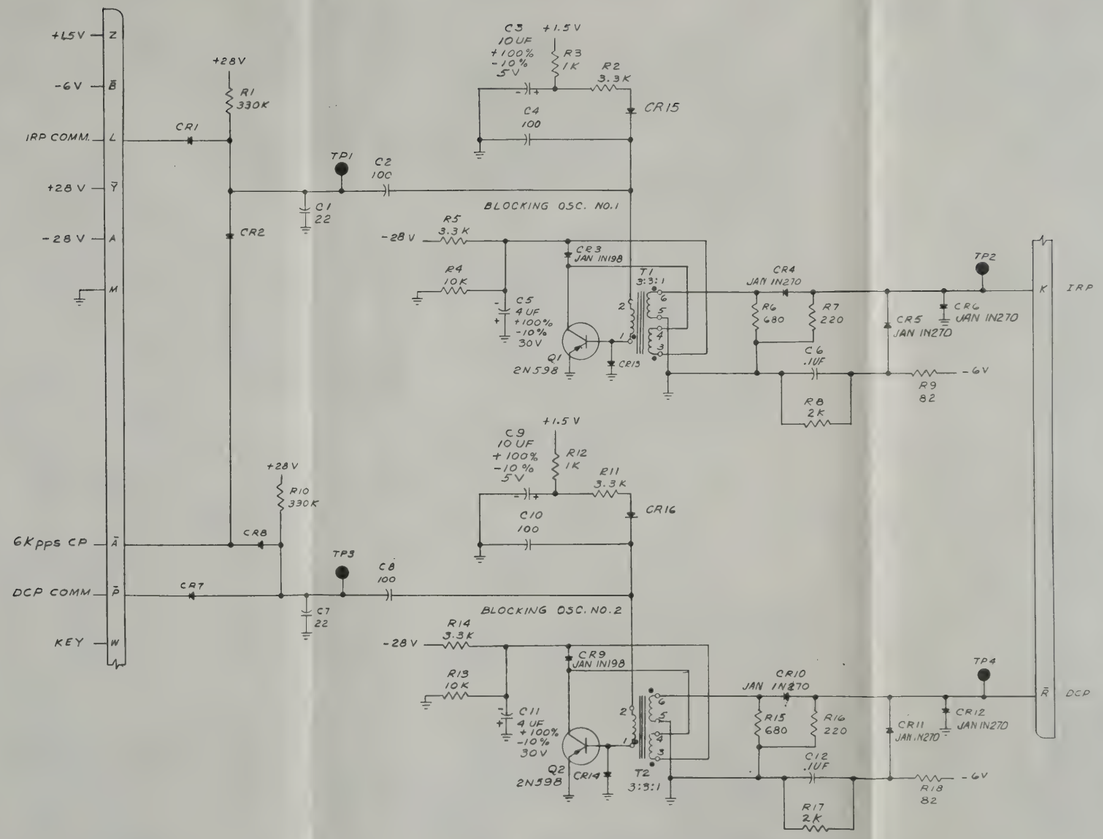


Figure 19. IRP and DCP generator 593982, schematic diagram.

6. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.
5. FOR ASSEMBLY SEE DWG. NO. 593982.
4. ALL DIODES ARE HD 2270.
3. ALL GROUNDS AND VOLTAGES ARE D.C.
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS ±10%, 100V. TOLERANCE AND VOLTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.
1. ALL RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT. TOLERANCE AND WATTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.

NOTES: (UNLESS OTHERWISE SPECIFIED)

USED ON THIS DRAWING			
COMPONENT	FIRST NUMBER	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C1	C12	NONE
DIODES	CR1	CR16	NONE
RESISTOR	R1	R18	NONE
TRANSISTOR	Q1	Q2	NONE
TRANSFORMER	T1	T2	NONE

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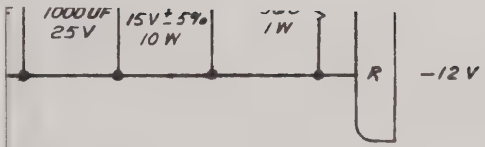
761-494 O - 63 - Fols. Text No. 14

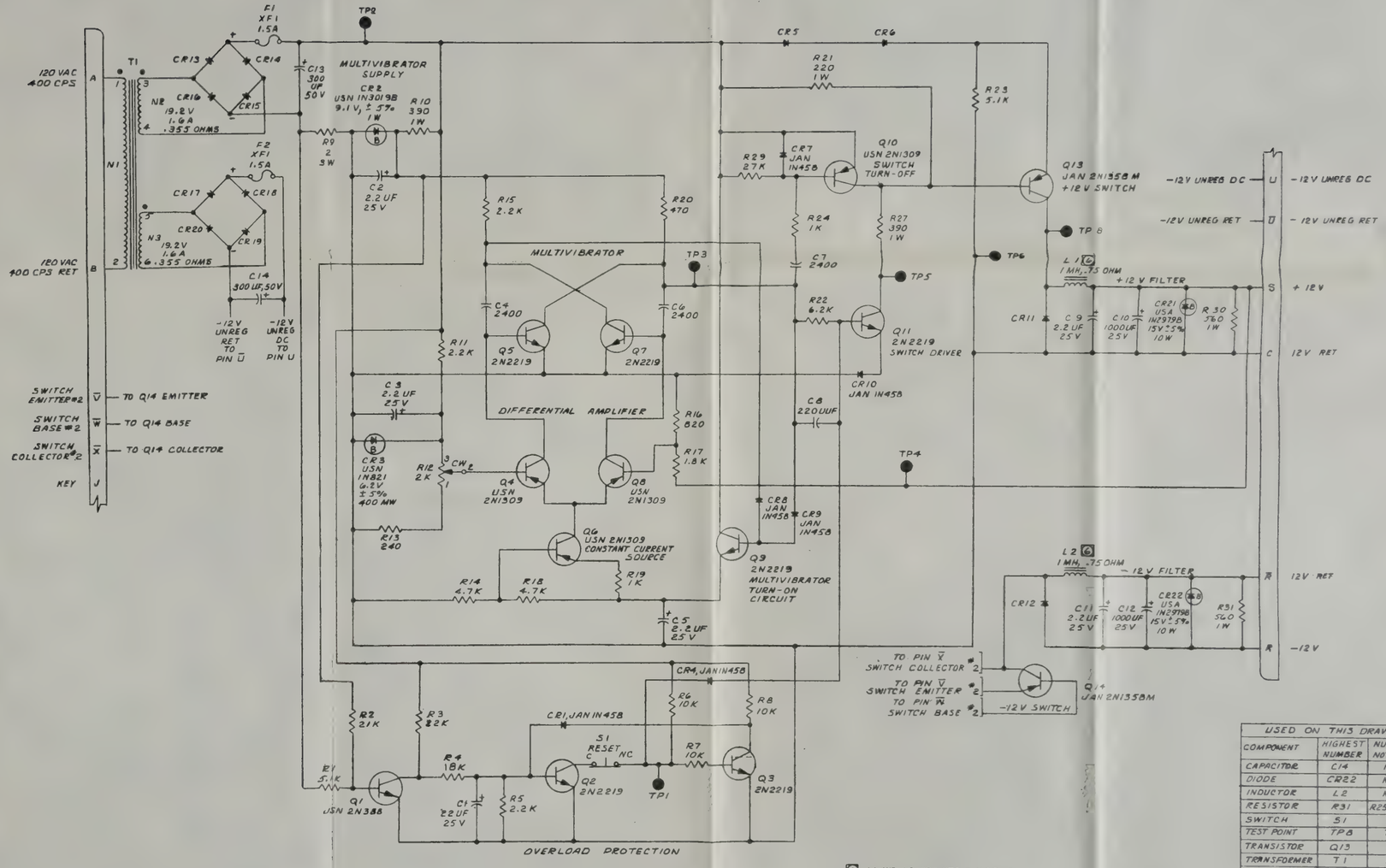


14
N 2N1358M

USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C14	NONE
DIODE	CR22	NONE
INDUCTOR	L2	NONE
RESISTOR	R31	R25, R26, R28
SWITCH	S1	NONE
TEST POINT	TP8	TP7
TRANSISTOR	Q13	Q12
TRANSFORMER	T1	NONE
FUSE	F2	NONE
FUSEHOLDER	XF1	NONE

10%, 50V.
T MIN. REQ.

T MIN. REQ.



USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C14	NONE
DIODE	CR22	NONE
INDUCTOR	L2	NONE
RESISTOR	R31	R25, R26, R28
SWITCH	S1	NONE
TEST POINT	TP8	TP7
TRANSISTOR	Q13	Q12
TRANSFORMER	T1	NONE
FUSE	F2	NONE
FUSEHOLDER	XF1	NONE

6. L1 AND L2 ARE UTC # MQD-0.
5. DIODES ARE 1N1563A.
4. T 1S 400 CPS, 1 Ø, 8% REGULATION POWER TRANSFORMER.
3. CAPACITANCE VALUES ARE IN MICROMICROFARADS ± 10%, 50V. TOLERANCE AND VOLTAGE DESIGNATED REPRESENT MIN. REQ.
2. RESISTANCE VALUES ARE IN OHMS ± 5% 1/2 WATT. TOLERANCE AND WATTAGE DESIGNATED REPRESENT MIN. REQ.
1. FOR ASSEMBLY SEE DWG NO. 1512530.

NOTES: (UNLESS OTHERWISE SPECIFIED)

TM5895-312-30-40

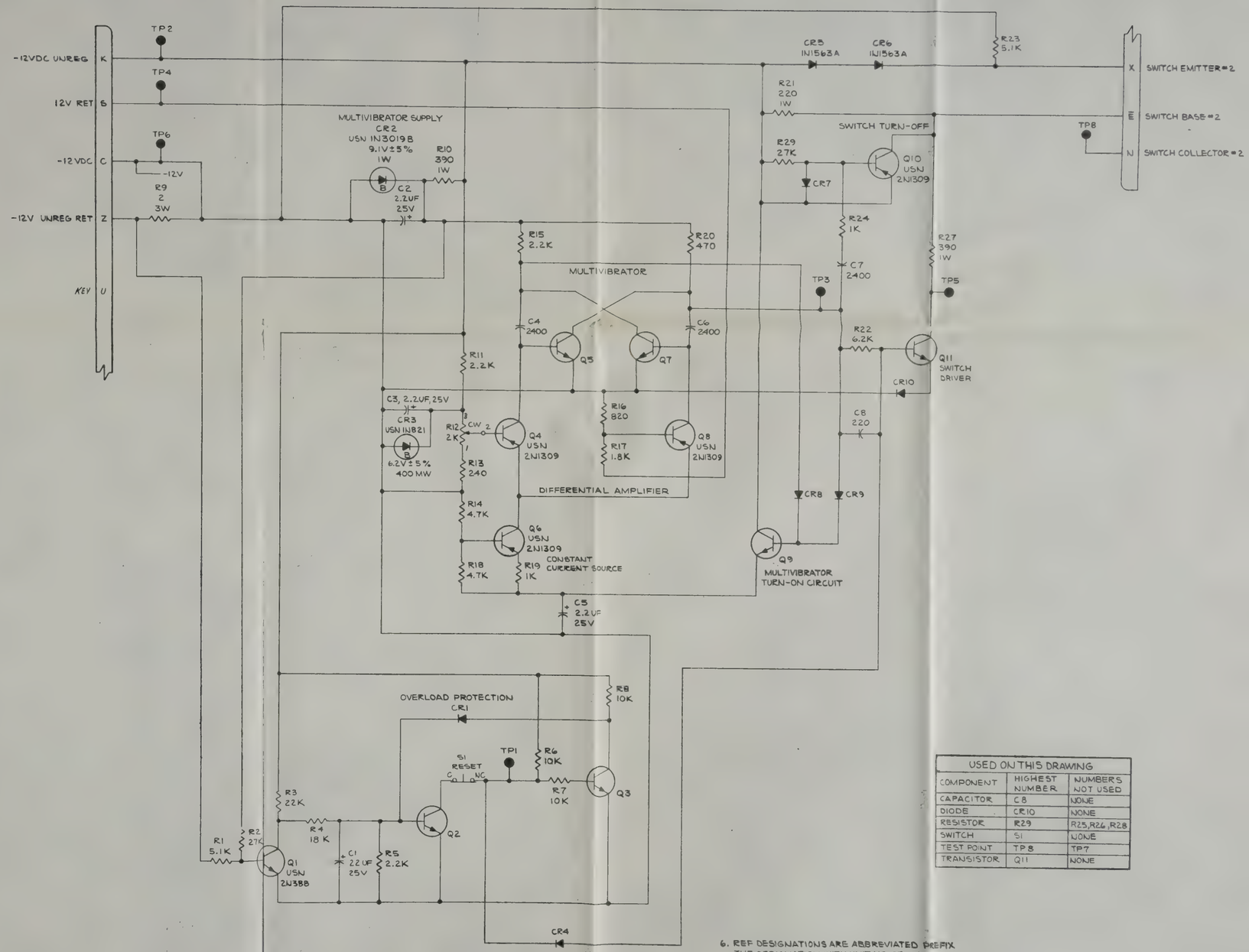
Figure 20. Power supply ±12-volt 1512530, schematic diagram.

USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C8	NONE
DIODE	CR10	NONE
RESISTOR	R29	R25,R26,R28
SWITCH	S1	NONE
TEST POINT	TP8	TP7
TRANSISTOR	Q11	NONE

REFIX
Y

RADS ± 10%, 300
MIN REQUIREMENTS.
2 WATT. TOL &
QUIREMENTS

TM 5895-312-30-41



USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C8	NONE
DIODE	CR10	NONE
RESISTOR	R29	R25, R26, R28
SWITCH	S1	NONE
TEST POINT	TP8	TP7
TRANSISTOR	Q11	NONE

6. REF DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATION WITH UNIT NO. OR ASSY DESIGNATION OR BOTH.
5. TRANSISTORS ARE TYPE 2N2219
4. DIODES ARE TYPE JAN,1N458
3. CAPACITANCE VALUES ARE IN MICROMICROFARADS ±10%, 300 VOLTS. TOL & VOLTAGE DESIGNATED REPRESENT MIN REQUIREMENTS
2. RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT. TOL & WATTAGE DESIGNATED REPRESENT MIN REQUIREMENTS
1. FOR ASSY SEE DWG NO. 1512552
NOTES: UNLESS OTHERWISE SPECIFIED

Figure 21. —12-volt regulator and —12-volt protector circuit 1512552, schematic diagram.

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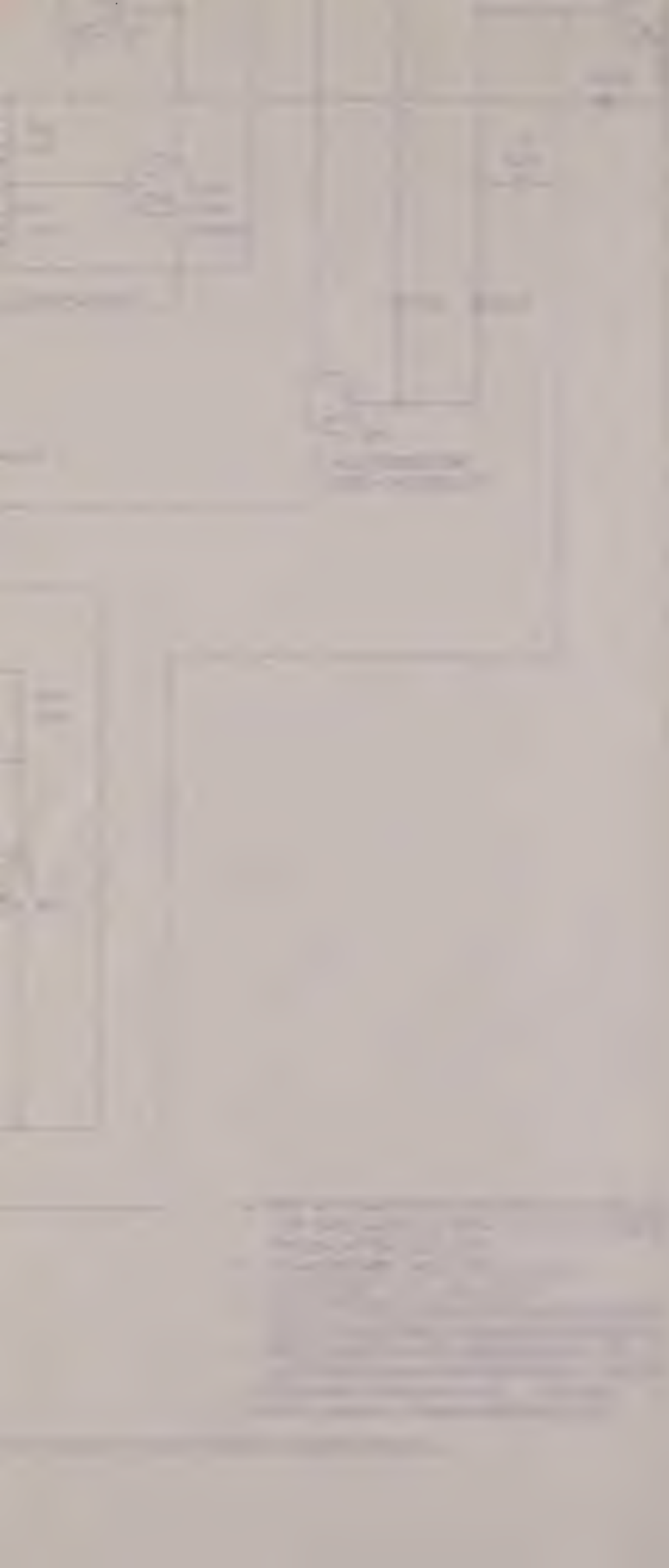
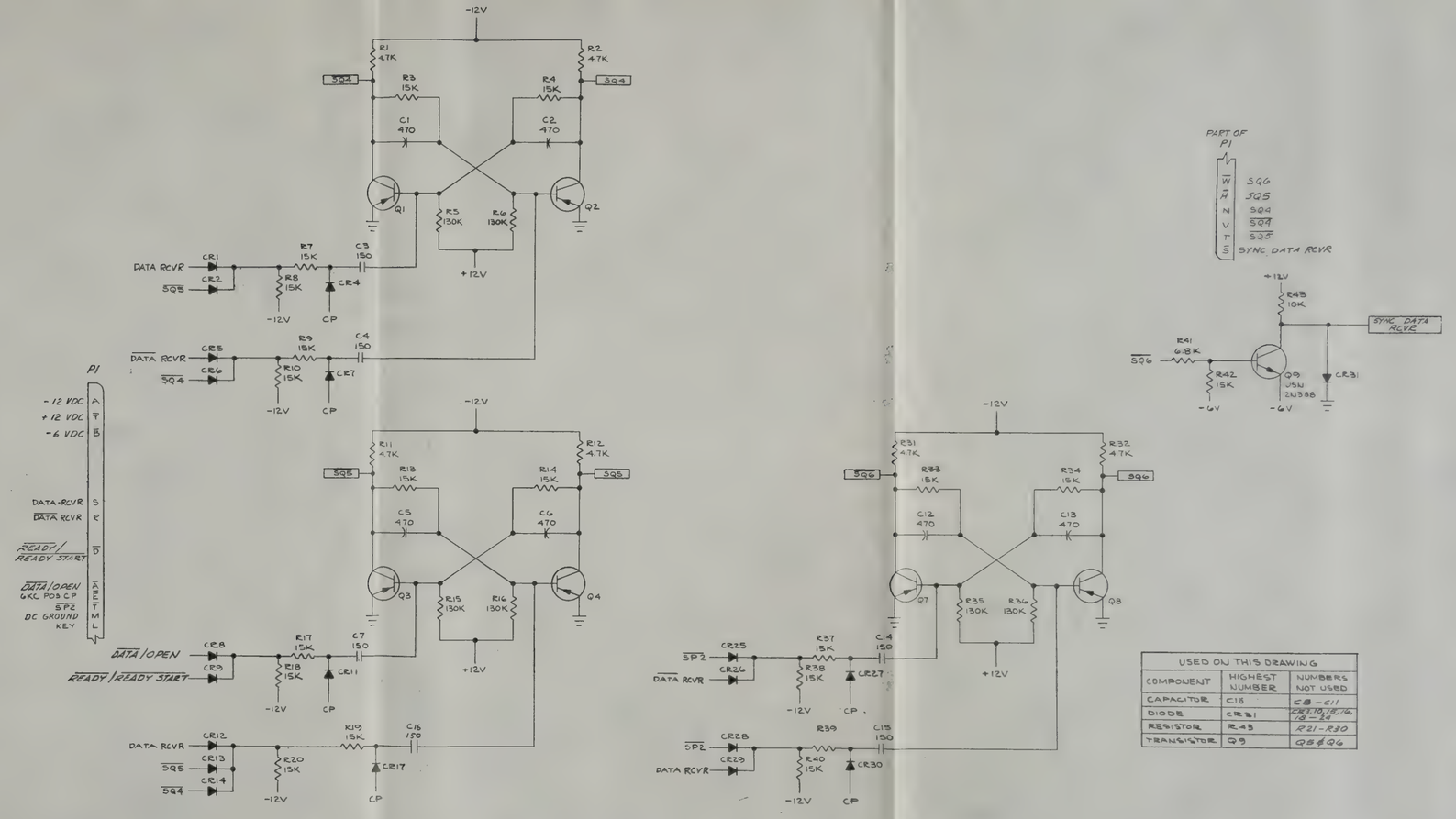
761-494 O - 65 - Fols. Text No. 17



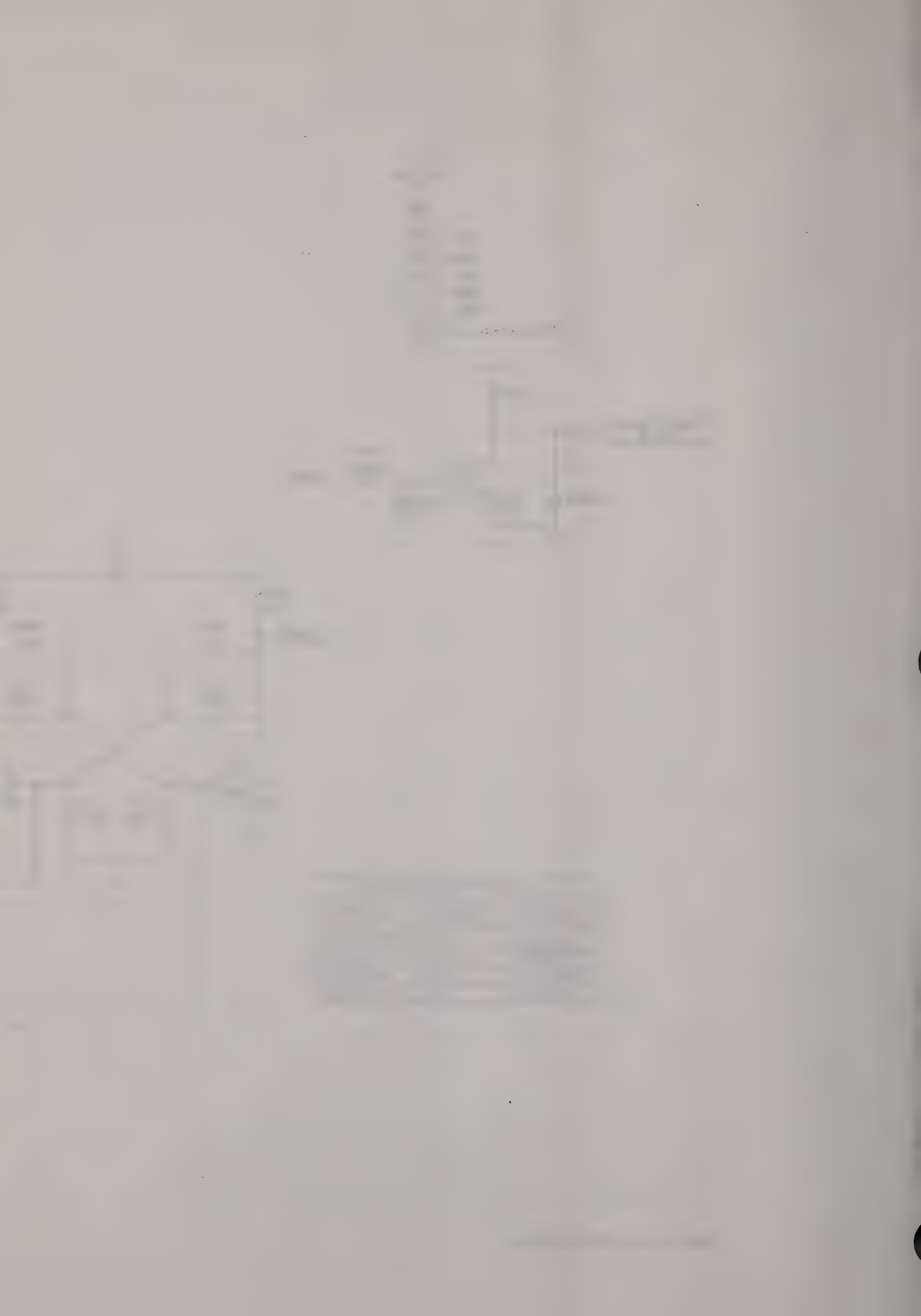


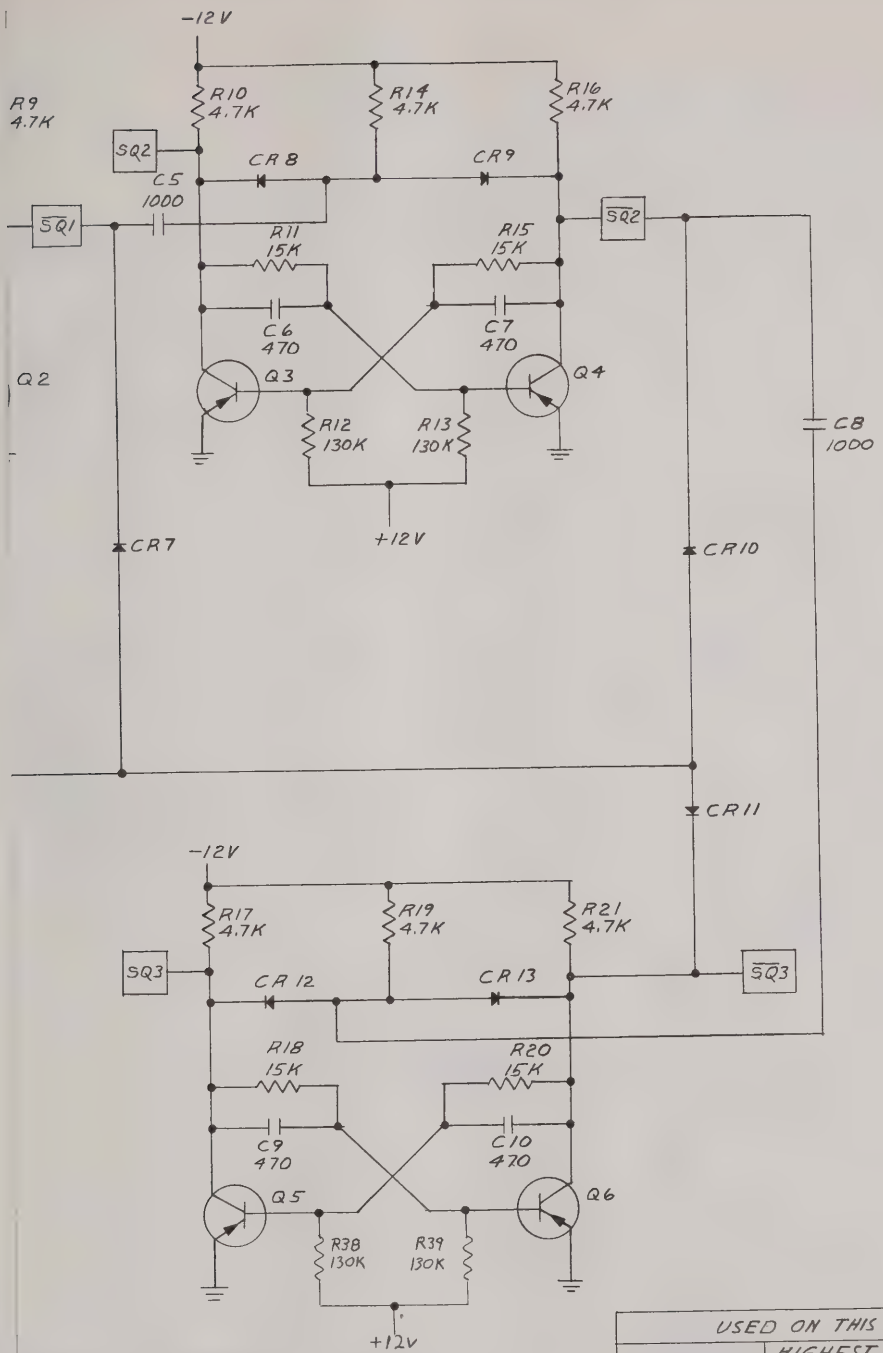
USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C18	C8 - C11
DIODE	CR31	CR3,10,15,16, 18 - 24
RESISTOR	R43	R21 - R30
TRANSISTOR	Q9	Q8 & Q6

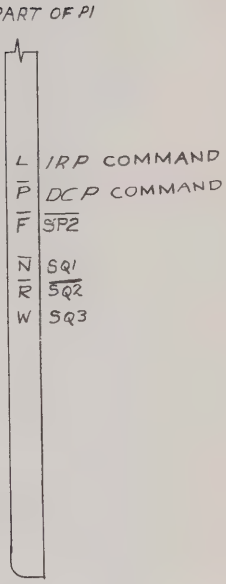
6. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NO. OR ASSY DESIGNATION OR BOTH.

5. TRANSISTORS ARE TYPE USAF 2N404.
4. DIODES ARE TYPE JAN 1N270
3. CAPACITANCE VALUES ARE IN PICOFARADS, ± 5%, 100 VOLT. TOL & VOLTAGE DESIGNATED REPRESENT MIN REQUIREMENTS.
2. RESISTANCE VALUES ARE IN OHMS ± 5%, ¼ WATT. TOL & WATTAGE DESIGNATED REPRESENT MIN REQUIREMENTS.
1. FOR ASSY SEE DWG NO. 1518302
NOTES: UNLESS OTHERWISE SPECIFIED

Figure 22. Synchronizer No. 1 1518320, schematic diagram.







USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C 10	NONE
DIODE	CR 19	NONE
RESISTOR	R 39	NONE
TRANSISTOR	Q 1	NONE

IATIONS ARE ABBREVIATED. PREFIX
WITH UNIT NO. OR ASSY DESIGNATION

TYPE USAF 2N404.

JAN 1N270

ES ARE IN PICOFARADS ± 5%,
LTAGE DESIGNATED REPRESENT
S.

ARE IN OHMS ± 5%, ¼ WATT. TOL &
TED REPRESENT MIN REQUIREMENTS.

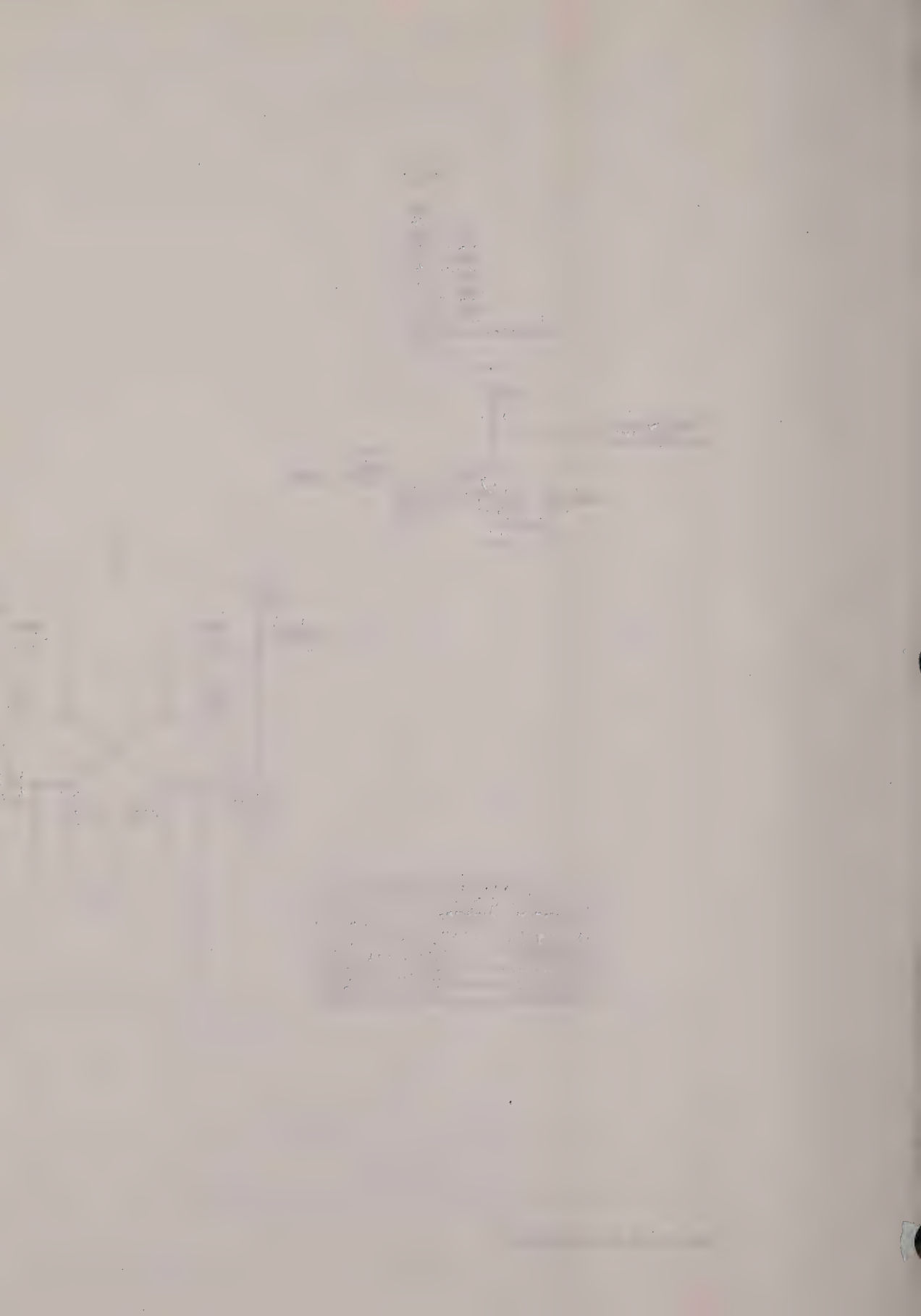
NO. 1518303.

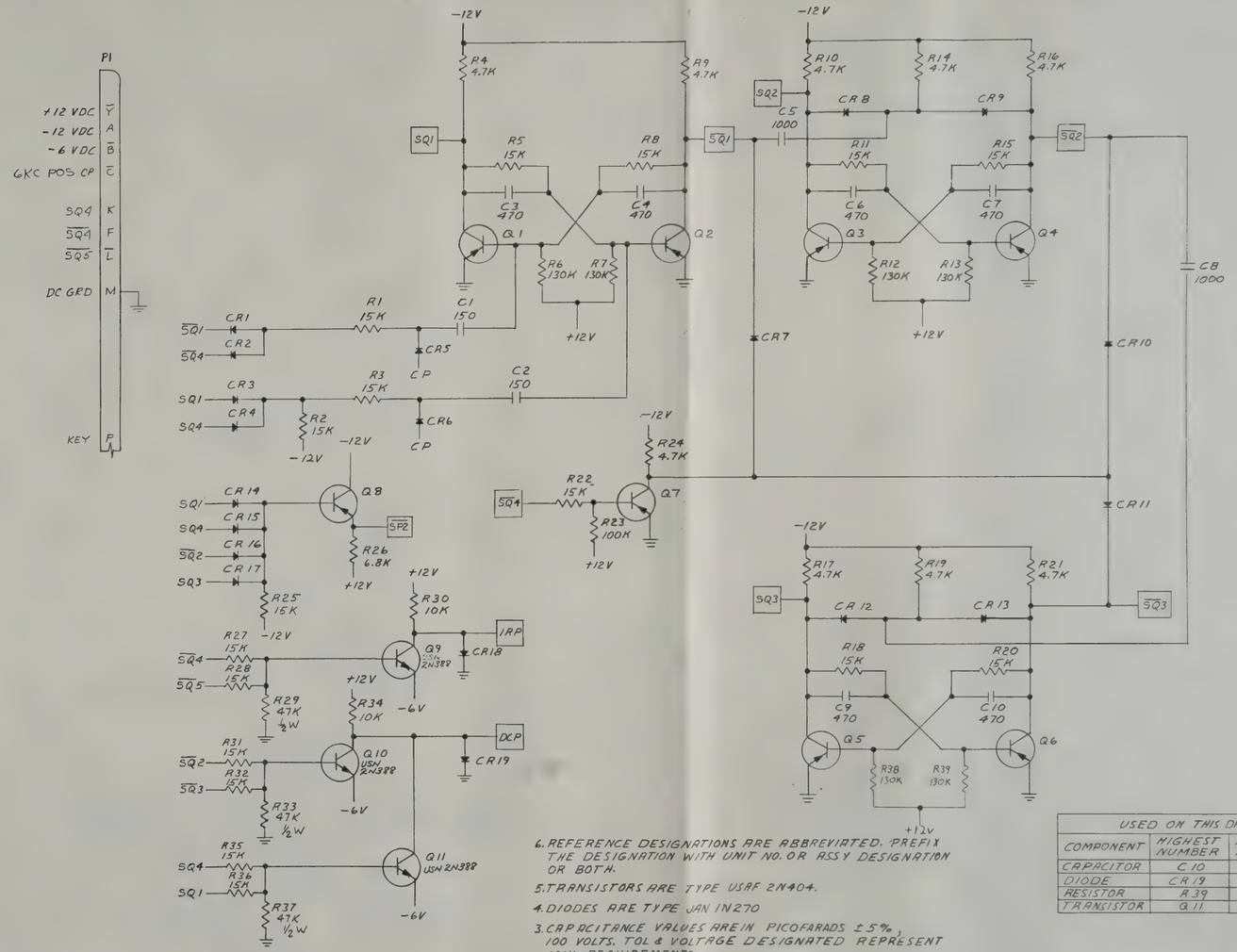
E SPECIFIED).

TM5895-312-30-C1-43

761-494 O - 65 - Fols. Text No. 18

No. 2 1518303, schematic diagram.





6. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NO. OR ASSY DESIGNATION OR BOTH.
5. TRANSISTORS ARE TYPE USAF 2N404.
4. DIODES ARE TYPE JAN 1N270
3. CAPACITANCE VALUES ARE IN PICOFARADS ±5%, 100 VOLTS. TOL & VOLTAGE DESIGNATED REPRESENT MIN REQUIREMENTS.
2. RESISTANCE VALUES ARE IN OHMS ± 5%, ¼ WATT. TOL & WATTAGE DESIGNATED REPRESENT MIN REQUIREMENTS.
1. FOR ASSY SEE DWG NO. 1518303.

NOTES: (UNLESS OTHERWISE SPECIFIED).

USED ON THIS DRAWING

COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C 10	NONE
DIODE	CR 19	NONE
RESISTOR	R 39	NONE
TRANSISTOR	Q 11	NONE

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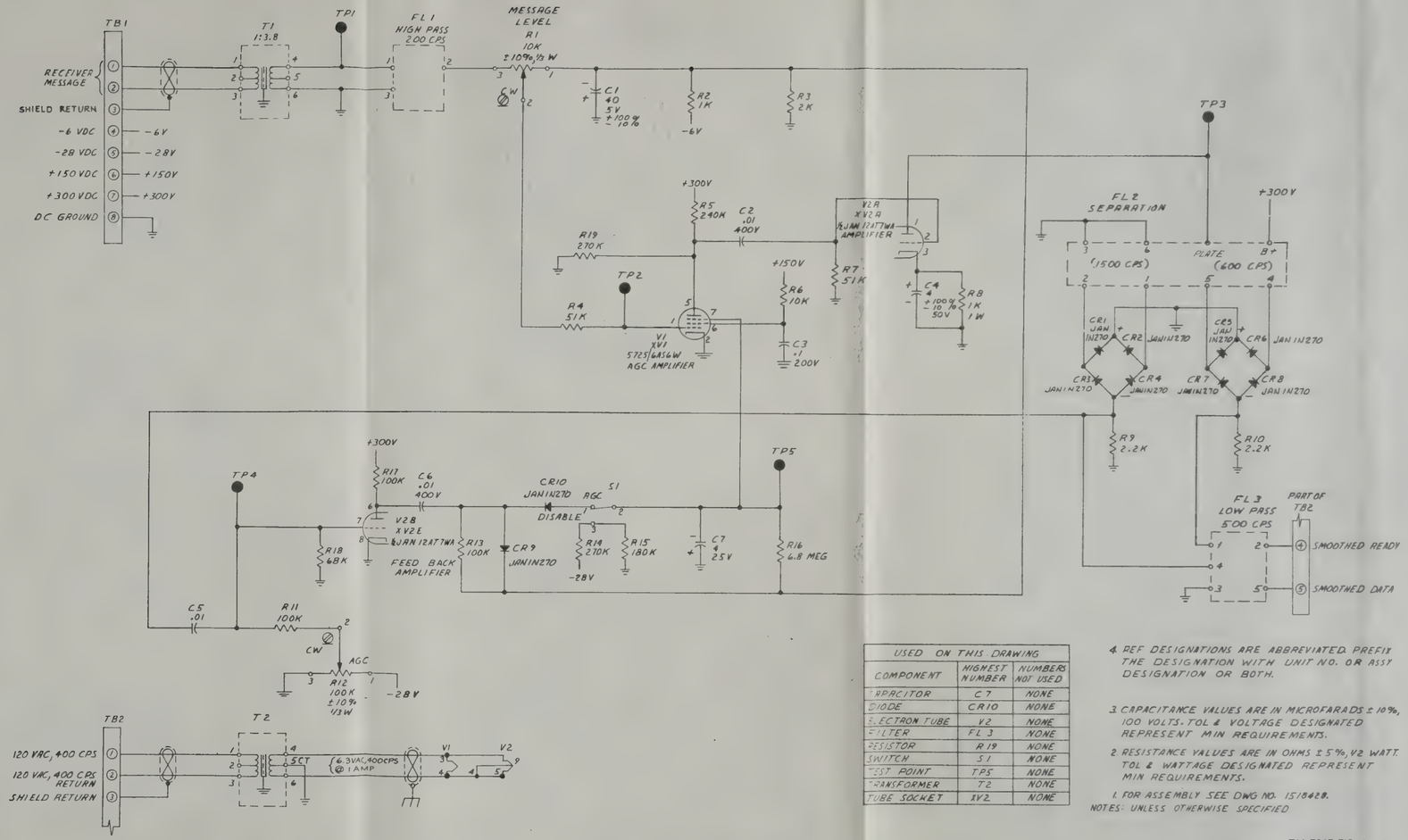
Figure 23. Synchronizer No. 2 1518303, schematic diagram.

761-494 O - 65 - Fols. Text No. 18

761-494 O - 65 - Fols. Text No. 19



USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C7	NONE
DIODE	CR10	NONE
ELECTRON TUBE	V2	NONE
FILTER	FL3	NONE
RESISTOR	R19	NONE
SWITCH	S1	NONE
TEST POINT	TP5	NONE
TRANSFORMER	T2	NONE
TUBE SOCKET	XV2	NONE

4. REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NO. OR ASSY DESIGNATION OR BOTH.

3. CAPACITANCE VALUES ARE IN MICROFARADS ± 10%, 100 VOLTS. TOL & VOLTAGE DESIGNATED REPRESENT MIN REQUIREMENTS.

2. RESISTANCE VALUES ARE IN OHMS ± 5%, ½ WATT. TOL & WATTAGE DESIGNATED REPRESENT MIN REQUIREMENTS.

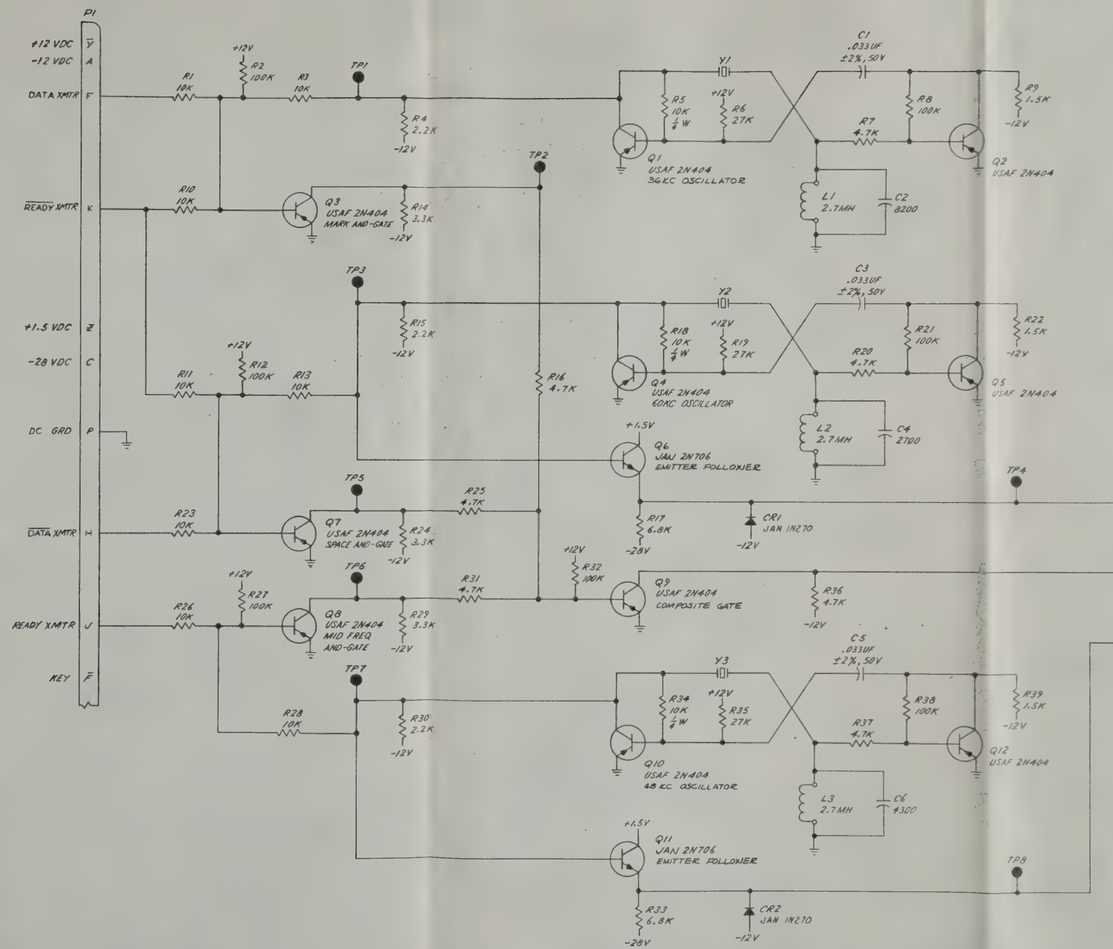
1. FOR ASSEMBLY SEE DWG NO. 1518428.

NOTES: UNLESS OTHERWISE SPECIFIED

TM 5895-312-30-44

Figure 24. Amplifier demodulator chassis 1518428, schematic diagram.

761-494 O - 65 - Fols. Text No. 20



USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C6	NONE
COIL	L3	NONE
CRYSTAL	Y3	NONE
RESISTOR	R39	NONE
TEST POINT	TP8	NONE
TRANSISTOR	Q12	NONE
DIODE	CR2	NONE

5. REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NO. OR ASSY DESIGNATION OR BOTH

4 FOR SIGNAL INFO SEE UNIT SCHEMATIC

3. CAPACITANCE VALUES ARE IN PICOFARADS ± 5%, 50 VOLTS. TOL & VOLTAGE DESIGNATED REPRESENT MIN REQUIREMENTS

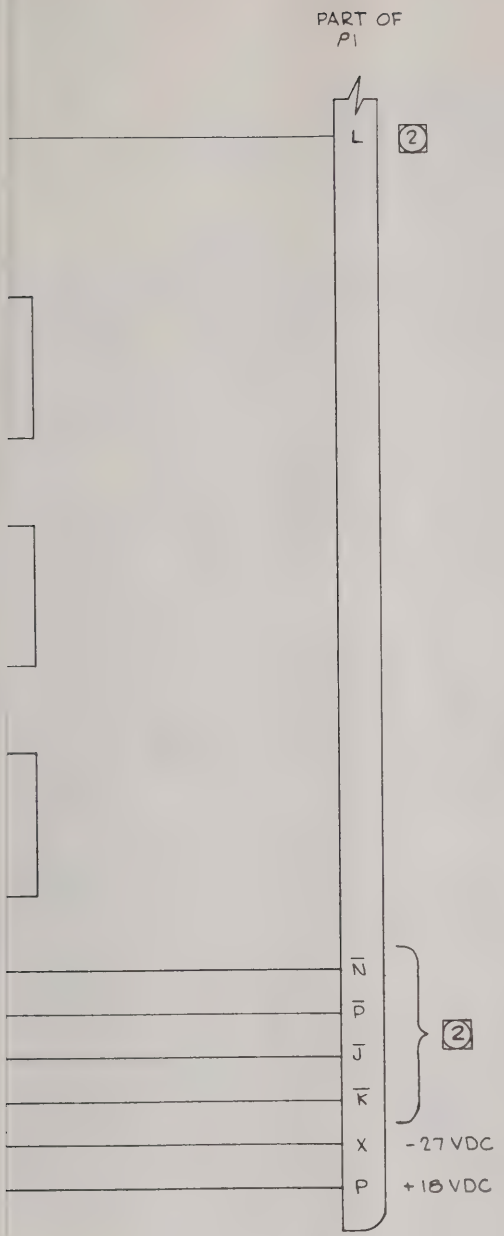
2. RESISTANCE VALUES ARE IN OHMS ±5%, 1/4 WATT. TOL & WATTAGE DESIGNATED REPRESENT MIN REQUIREMENTS

1. FOR ASSY SEE DWG NO. 1518471.

NOTES: UNLESS OTHERWISE SPECIFIED

TM 5895-312-30-45

Figure 25. Modulator gate and oscillator 1518471, schematic diagram.



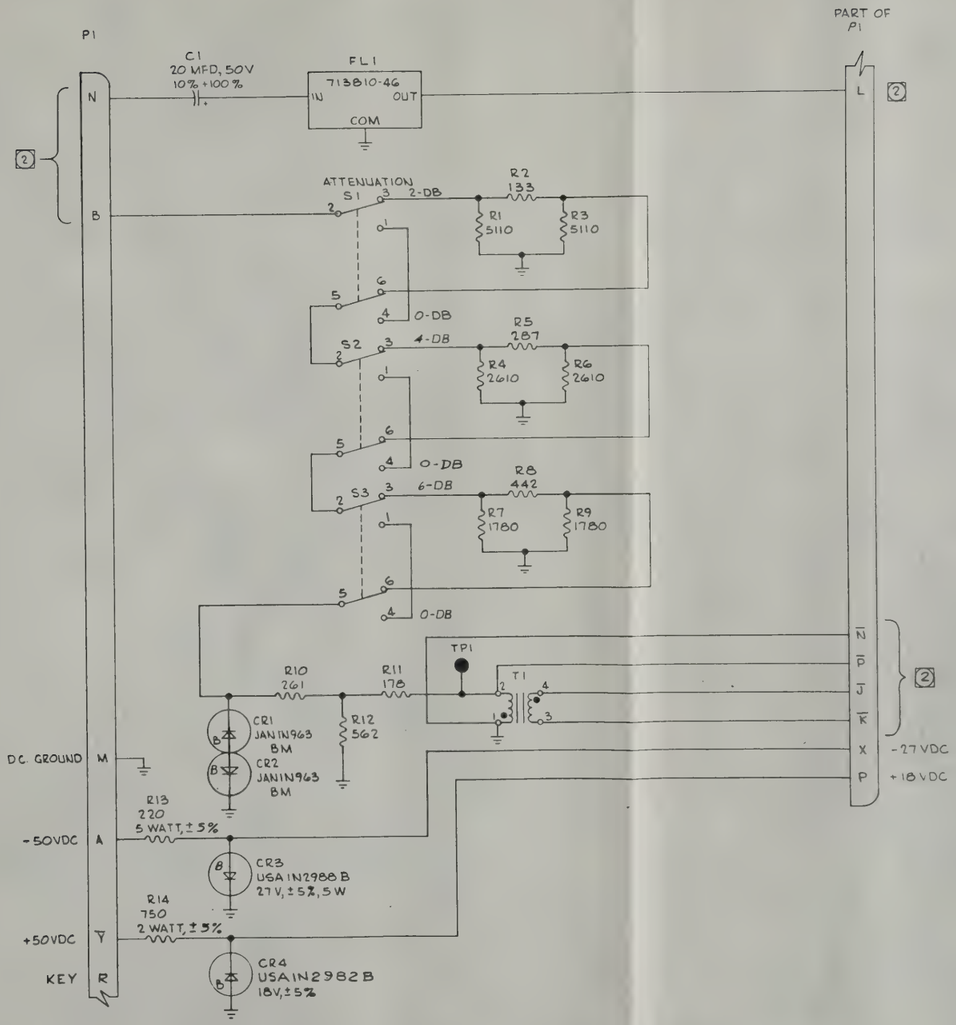
USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C1	NONE
DIODE	CR4	NONE
FILTER	FL1	NONE
RESISTOR	R14	NONE
SWITCH	S3	NONE
TEST POINT	TP1	NONE
TRANSFORMER	T1	NONE

5. CAPACITANCE TOLERANCE AND VOLTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.
4. FOR ASSEMBLY DWG SEE 1518484.
3. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.
2. FOR SIGNAL INFORMATION SEE UNIT SCHEMATIC.
1. ALL RESISTANCE VALUES ARE IN OHMS ± 1%, ¼ WATT, TOLERANCE AND WATTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.

NOTES: (UNLESS OTHERWISE SPECIFIED).

Modulator output 1518484, schematic diagram.

761-494 O - 65 - Fols. Text No. 21



USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C1	NONE
DIODE	CR4	NONE
FILTER	FL1	NONE
RESISTOR	R14	NONE
SWITCH	S3	NONE
TEST POINT	TP1	NONE
TRANSFORMER	T1	NONE

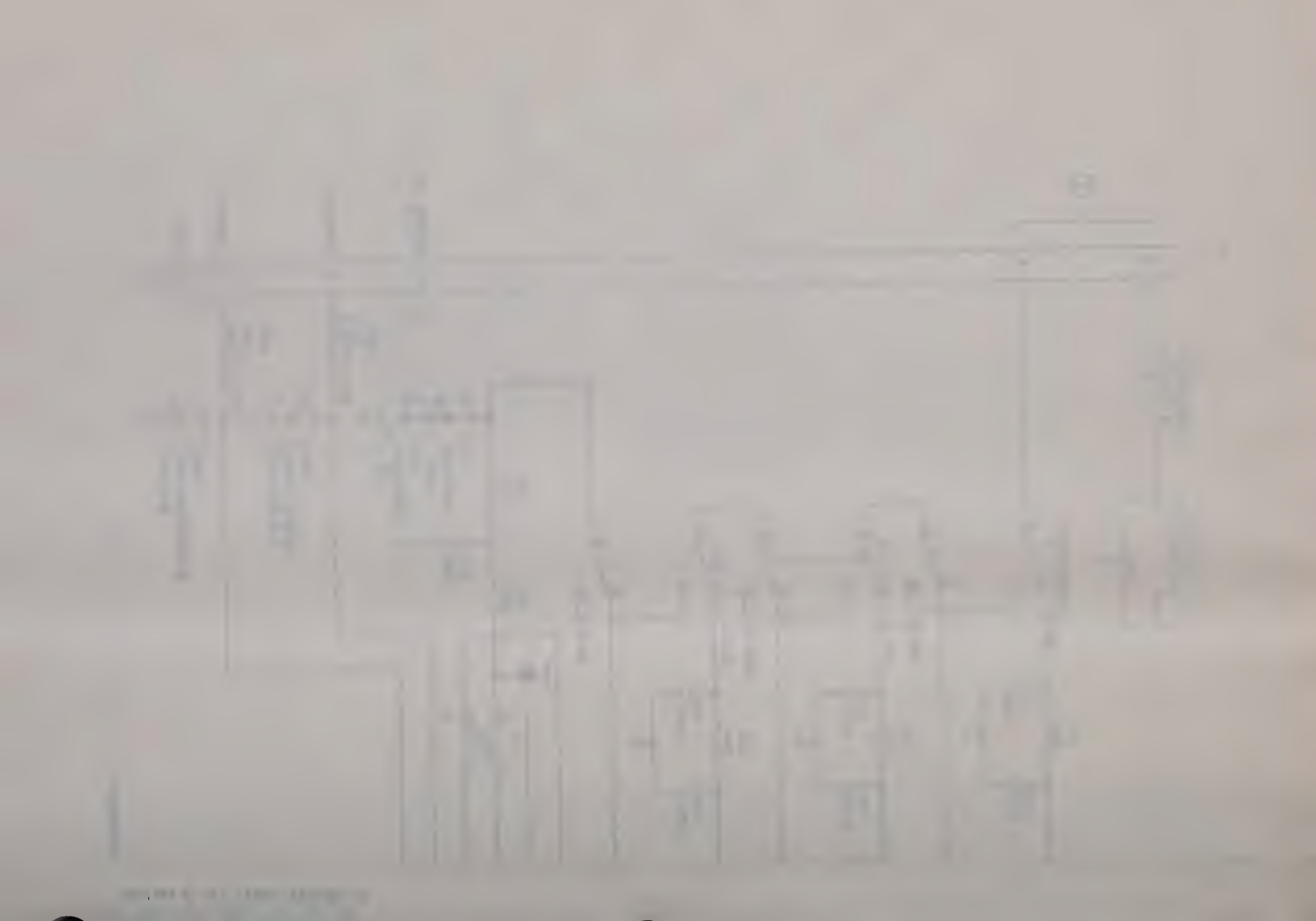
5. CAPACITANCE TOLERANCE AND VOLTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.
4. FOR ASSEMBLY DWG SEE 1518484.
3. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH
2. FOR SIGNAL INFORMATION SEE UNIT SCHEMATIC
1. ALL RESISTANCE VALUES ARE IN OHMS ± 1%, ¼ WATT, TOLERANCE AND WATTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.

NOTES: (UNLESS OTHERWISE SPECIFIED).

TM 5895-312-30-46

Figure 26. Modulator output 1518484, schematic diagram.

761-494 O - 65 - Fols. Text No. 21



THIS DRAWING	
HIGHEST NUMBER	NUMBERS NOT USED
C2	NONE
CR12	NONE
R52	NONE
RT2	NONE
TPB 6	NONE
Q14	NONE

5. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH

(4) FOR SIGNAL INFORMATION SEE UNIT SCHEMATIC

3. CAPACITANCE VALUES ARE IN MICROFARADS ± 10 %, 100 VOLTS. TOL & VOLTAGE DESIGNATED REPRESENT MIN REQUIREMENTS.

2. RESISTANCE VALUES ARE OHMS ± 5 %, ½ WATT. TOL & WATTAGE DESIGNATED REPRESENT MIN REQUIREMENTS.

1. FOR ASSY SEE DWG NO. 1518486

NOTES: UNLESS OTHERWISE SPECIFIED

TM5895-312-30-48
FIG.28 1518486-200

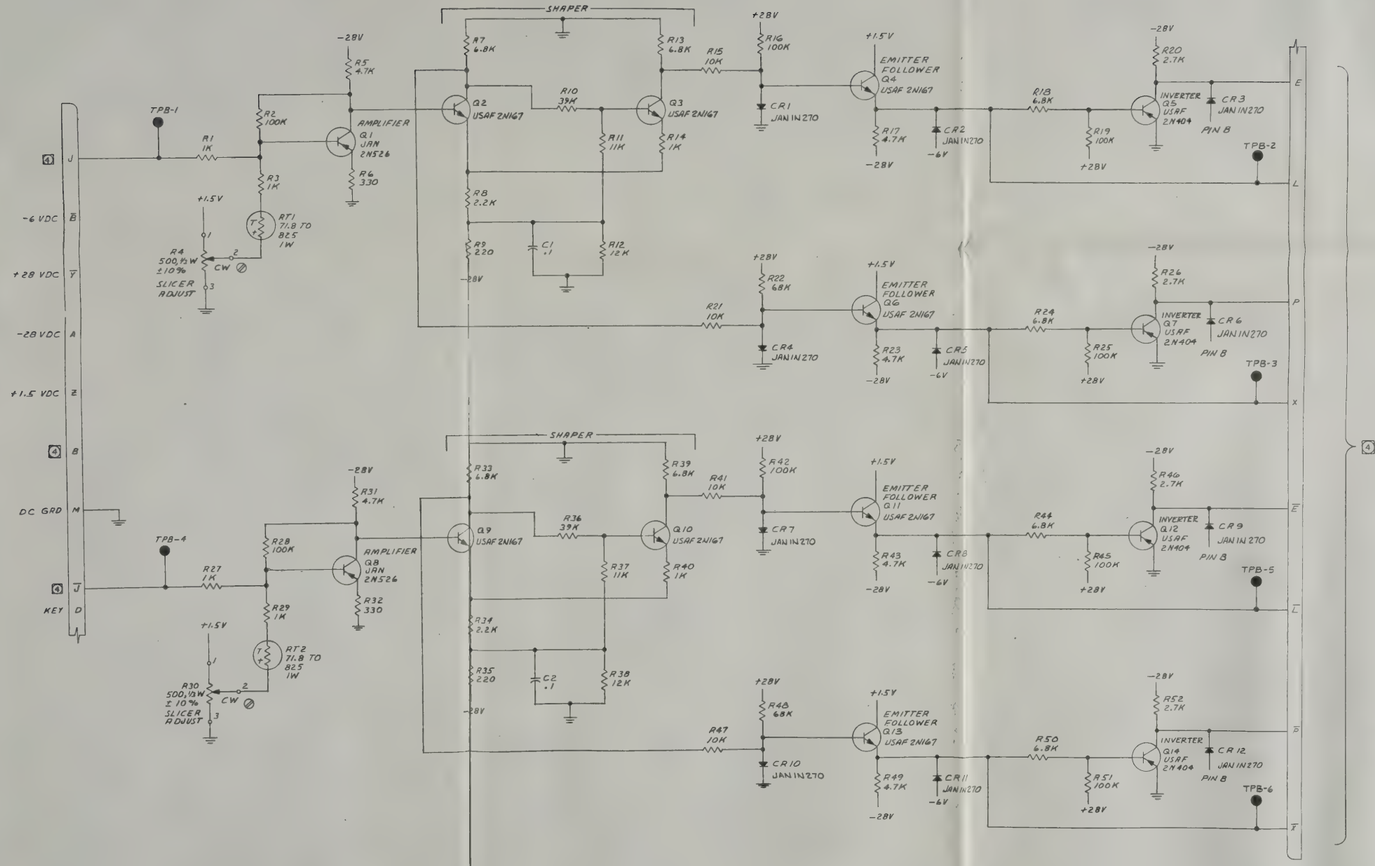


Figure 27. Slicer 1518186. schematic diagram.

USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C2	NONE
DIODE	CR12	NONE
RESISTOR	R52	NONE
RESISTOR, THERMAL	RT2	NONE
TEST POINT	TPB 6	NONE
TRANSISTOR	Q14	NONE

5. REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH

4 FOR SIGNAL INFORMATION SEE UNIT SCHEMATIC

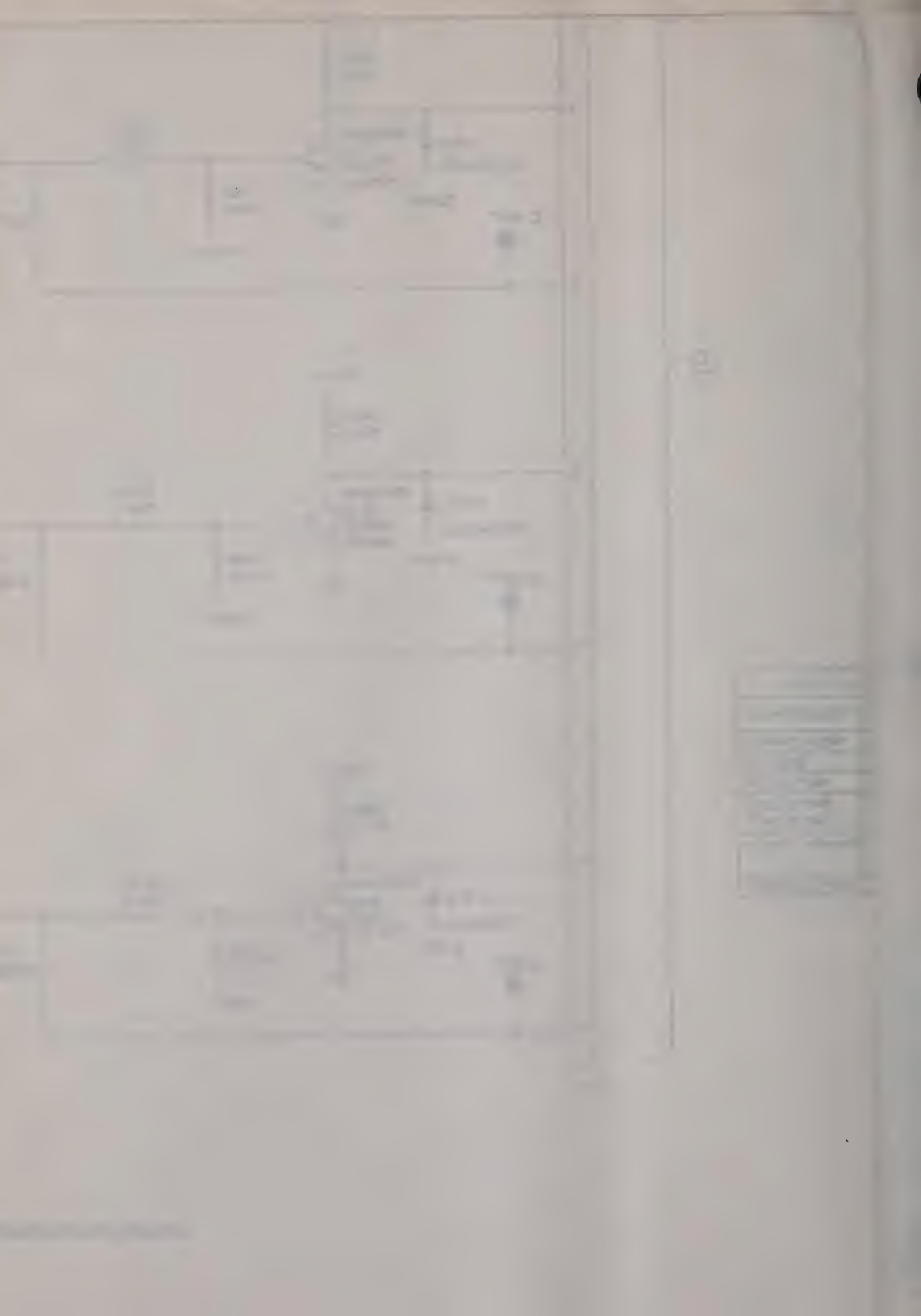
3 CAPACITANCE VALUES ARE IN MICROFARADS ± 10 %, 100 VOLTS. TOL & VOLTAGE DESIGNATED REPRESENT MIN REQUIREMENTS.

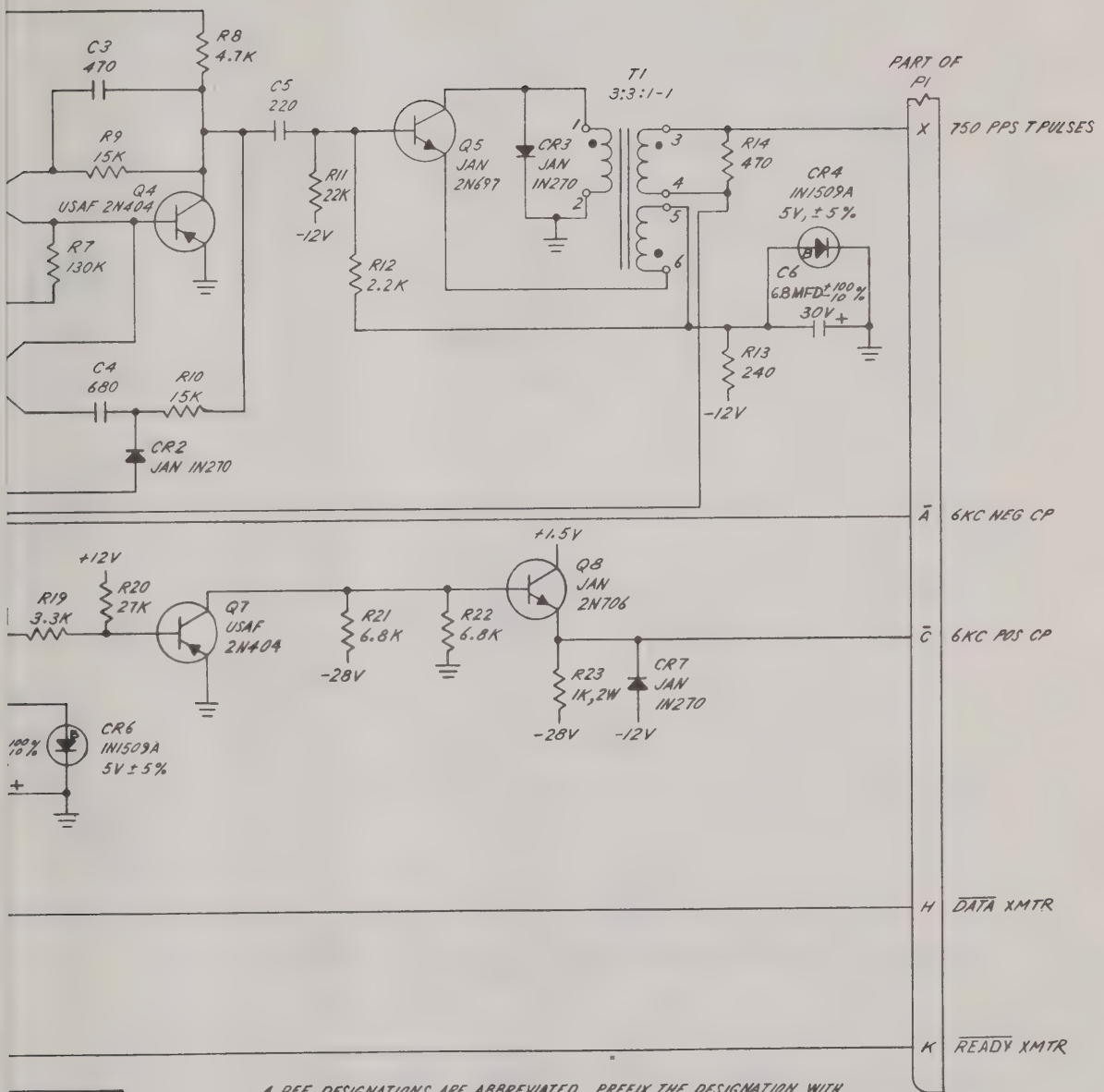
2 RESISTANCE VALUES ARE OHMS ± 5 %, 1/2 WATT. TOL & WATTAGE DESIGNATED REPRESENT MIN REQUIREMENTS

1. FOR ASSY SEE DWG NO. 1518486

NOTES: UNLESS OTHERWISE SPECIFIED

TM5895-312-30-48
FIG 28 1518486-200





DRAWING
NUMBERS
NOT USED
NONE
NONE
NONE
NONE
NONE

4. REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NO. OR ASSY DESIGNATION OR BOTH

3. CAPACITANCE VALUES ARE IN PICOFARADS ± 5%, 100 VOLTS. TOL & VOLTAGE DESIGNATED REPRESENT MIN REQUIREMENTS

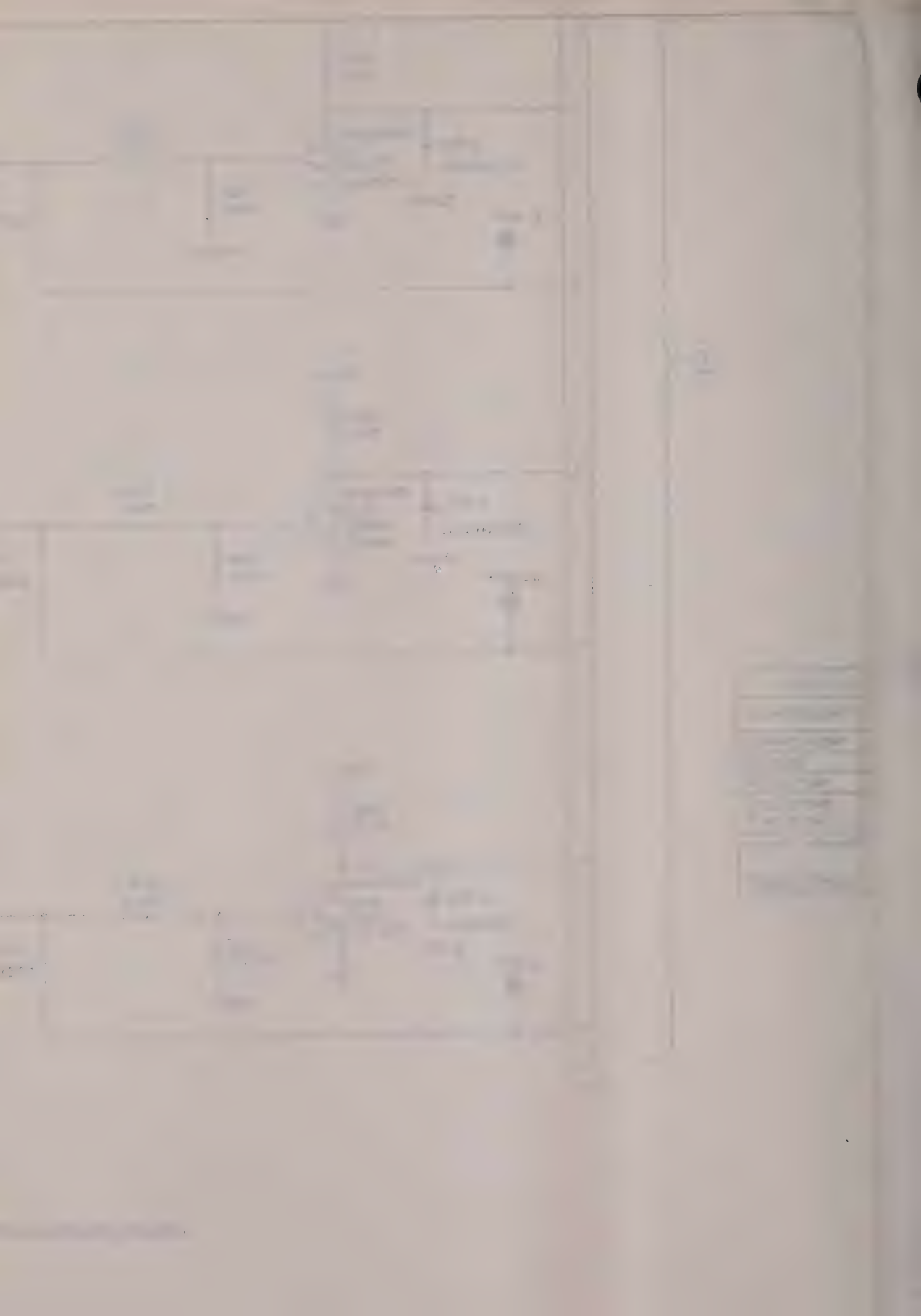
2. RESISTANCE VALUES ARE IN OHMS ± 5%, ½ WATT. TOL & WATTAGE DESIGNATED REPRESENT MIN REQUIREMENTS

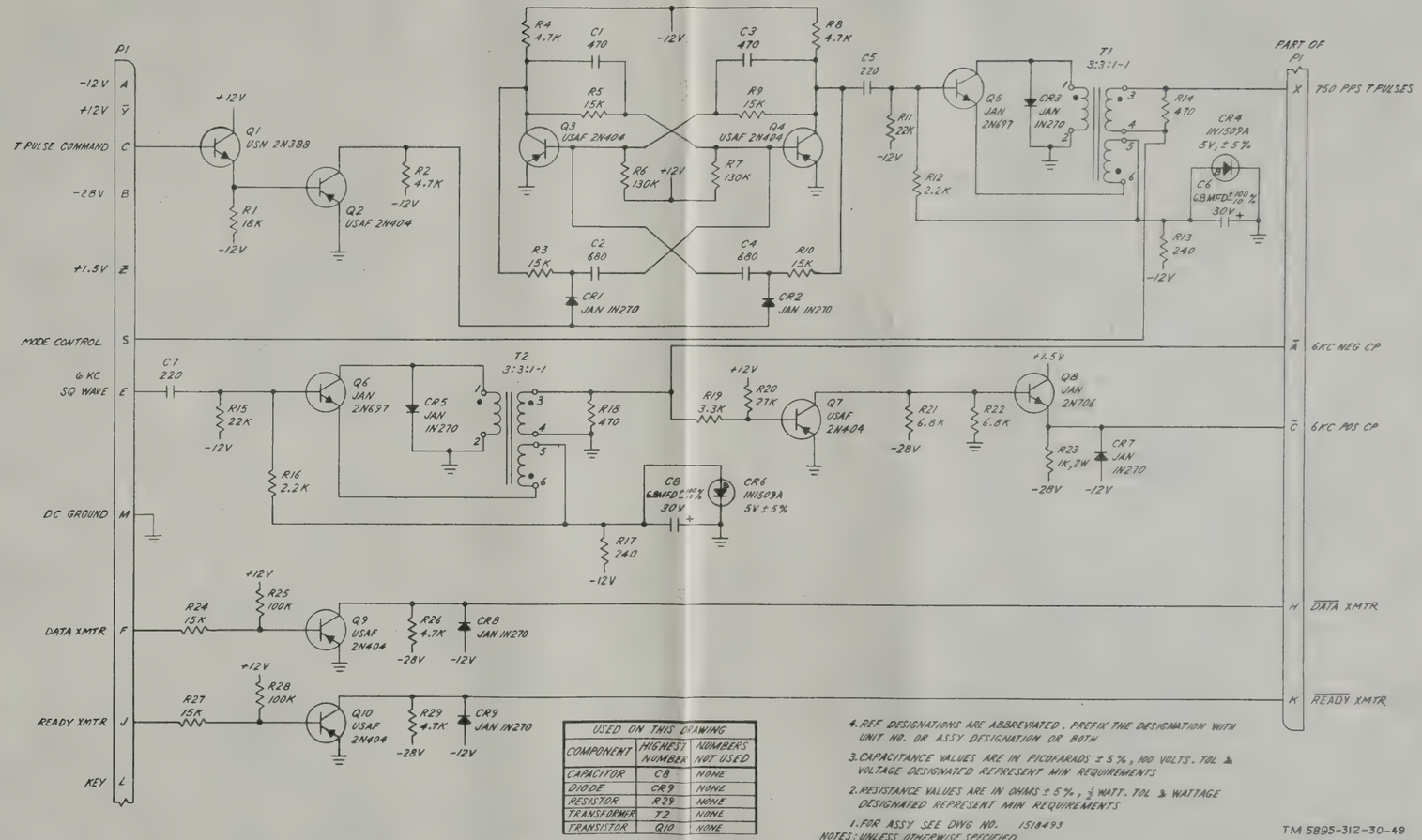
1. FOR ASSY SEE DWG NO. 1518493

NOTES: UNLESS OTHERWISE SPECIFIED

TM 5895-312-30-49

generator 1518493, schematic diagram.





USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C8	NONE
DIODE	CR9	NONE
RESISTOR	R29	NONE
TRANSFORMER	T2	NONE
TRANSISTOR	Q10	NONE

4. REF. DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NO. OR ASSY DESIGNATION OR BOTH

3. CAPACITANCE VALUES ARE IN PICOFARADS ± 5%, 100 VOLTS. TOL & VOLTAGE DESIGNATED REPRESENT MIN REQUIREMENTS

2. RESISTANCE VALUES ARE IN OHMS ± 5%, ½ WATT. TOL & WATTAGE DESIGNATED REPRESENT MIN REQUIREMENTS

1. FOR ASSY SEE DWG NO. 1518493

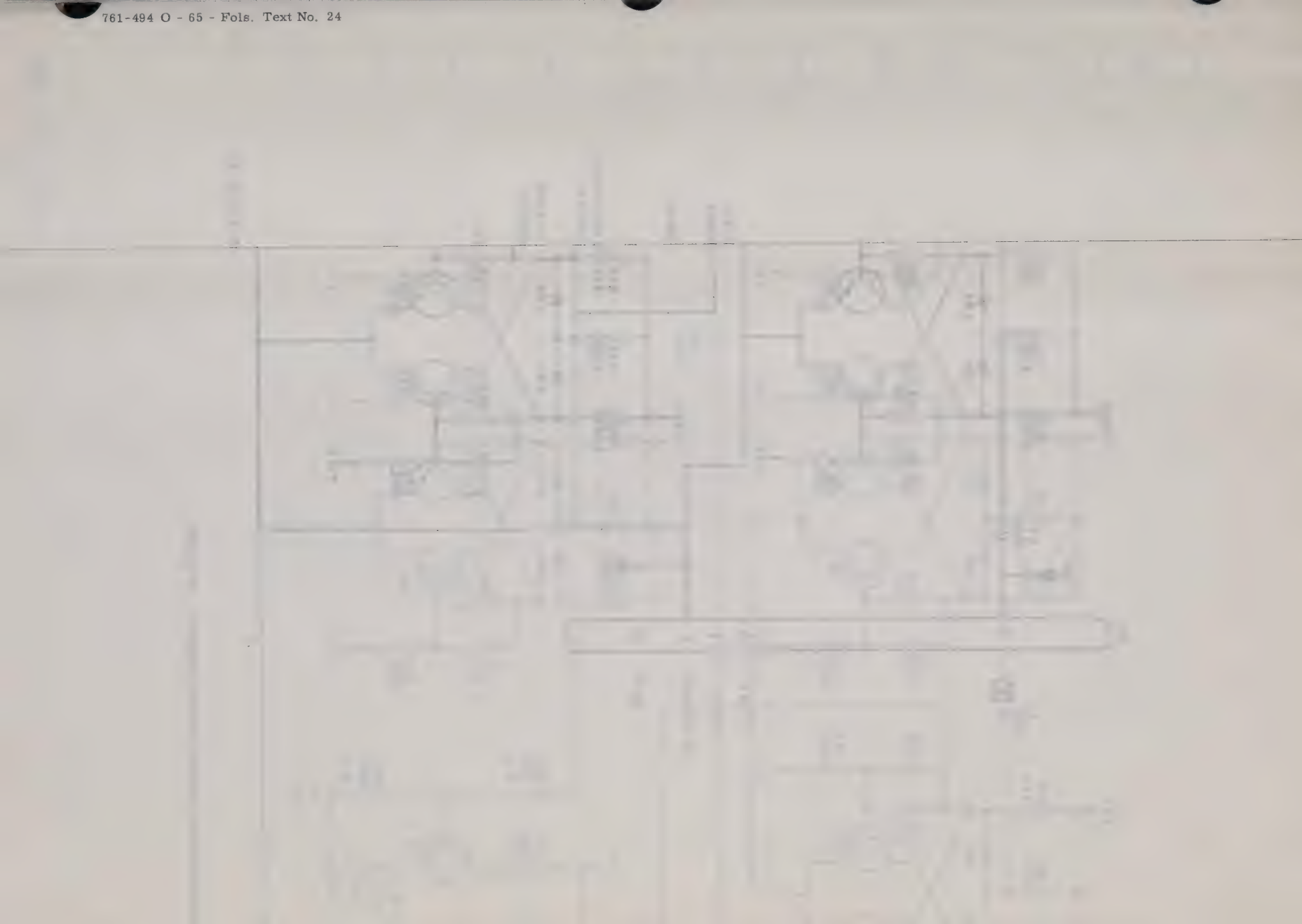
NOTES: UNLESS OTHERWISE SPECIFIED

TM 5895-312-30-49

Figure 28. 6-kc and 750-pps CP generator 1518493, schematic diagram.

761-494 O - 65 - Fols. Text No. 23

761-494 O - 65 - Fols. Text No. 24



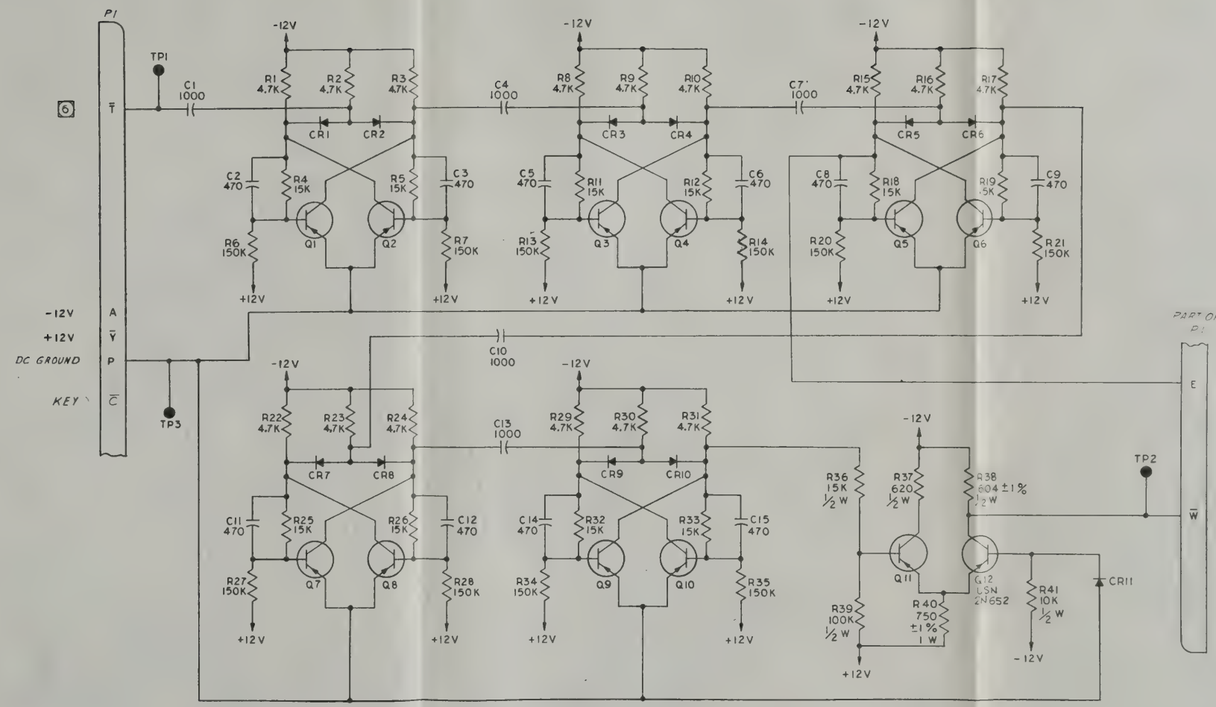


Figure 29. Frequency divider 1518494, schematic diagram.

7. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.
6. FOR SIGNAL INFORMATION SEE UNIT SCHEMATIC.
5. DIODES ARE TYPE JAN 1N276.
4. TRANSISTORS ARE TYPE USAF 2N404.
3. CAPACITANCE VALUES ARE IN PICOFARADS ±5%, 300 VOLTS. TOLERANCE AND VOLTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.
2. RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT. TOLERANCE AND WATTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.
1. FOR ASSEMBLY SEE DRAWING NO. 1518494.

NOTES: UNLESS OTHERWISE SPECIFIED

USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C15	NONE
DIODE	CR11	NONE
RESISTOR	R41	NONE
TEST POINT	TP3	NONE
TRANSISTOR	Q12	NONE

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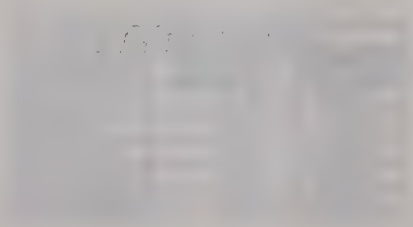
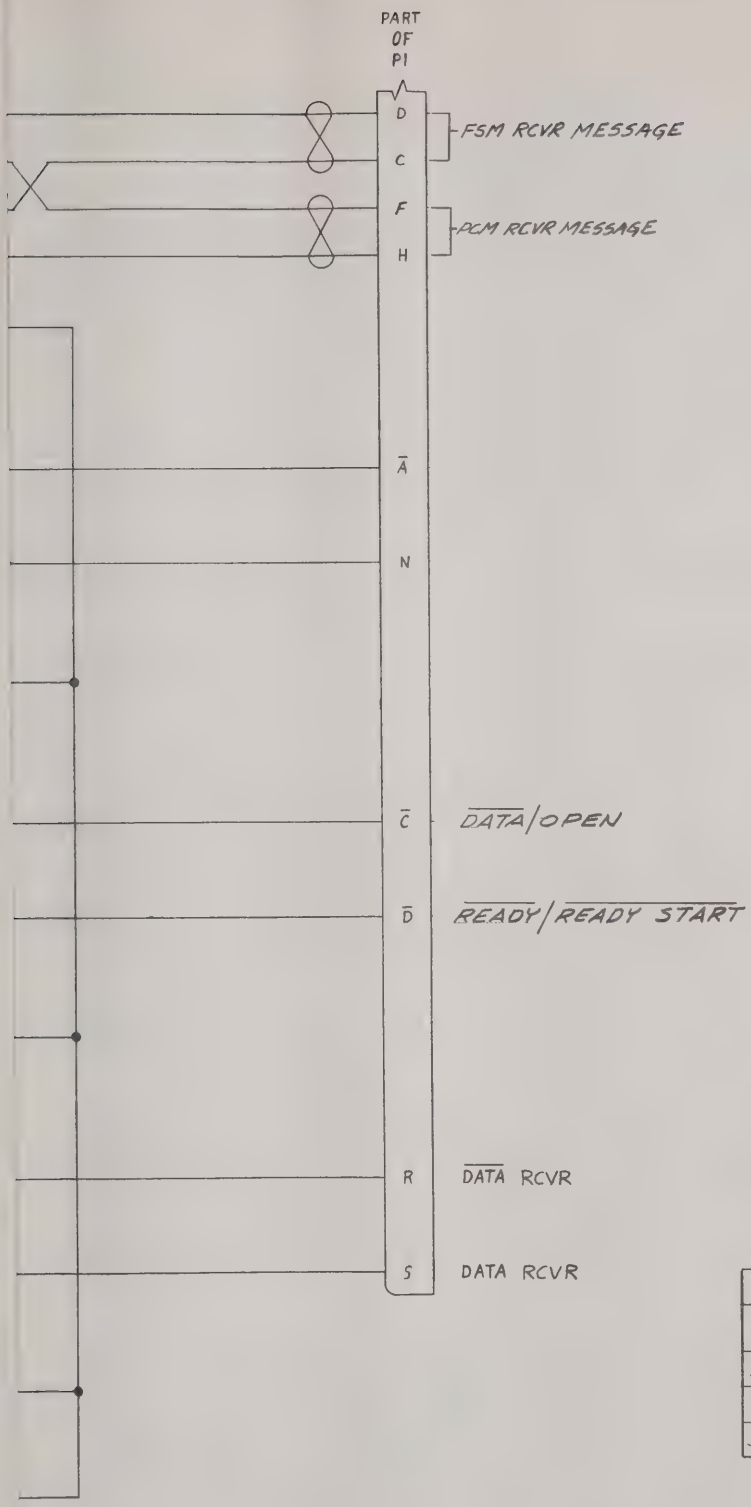




USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
DIODE	CR1	NONE
RELAY	K4	NONE
SWITCH	S1	NONE

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.

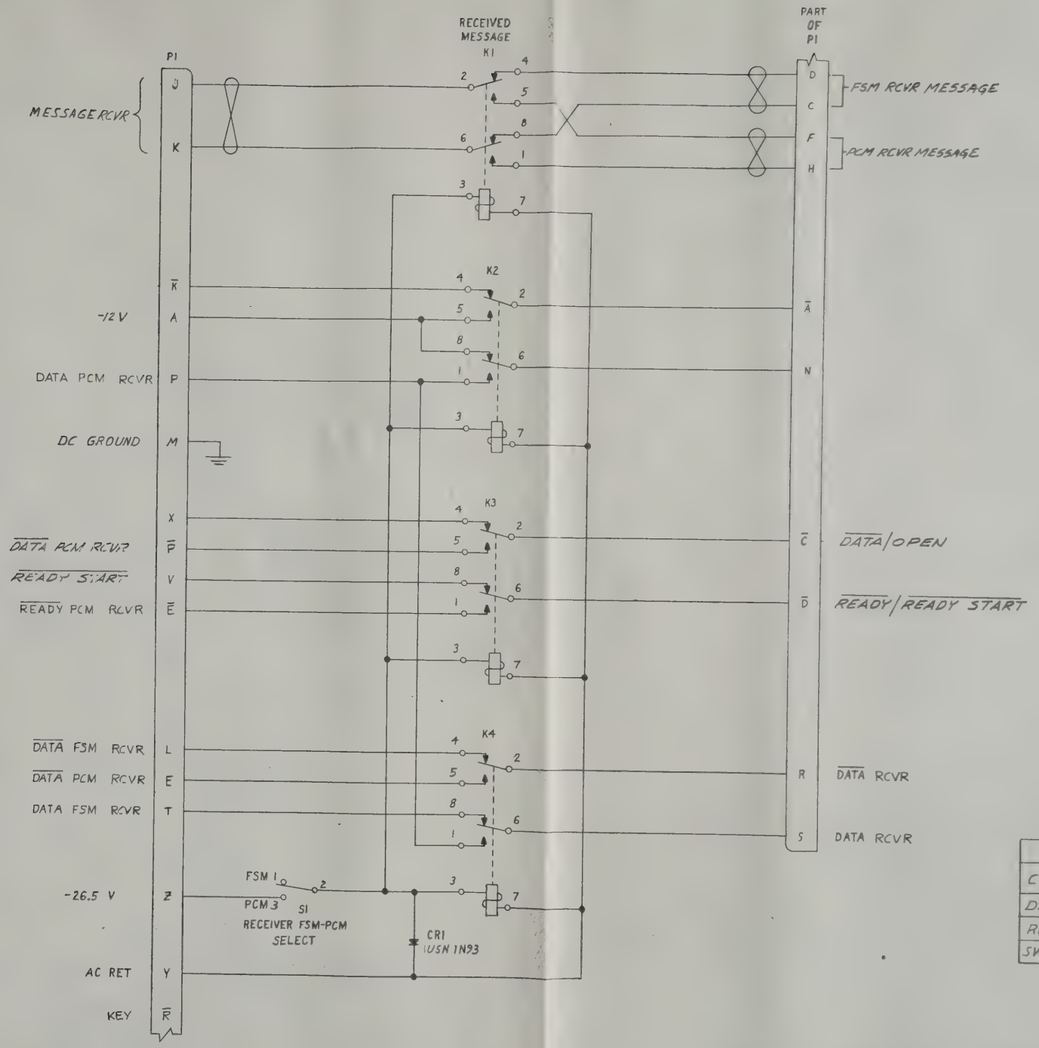
1. FOR ASSEMBLY SEE DRAWING NO. 1522307

NOTES: UNLESS OTHERWISE SPECIFIED

TM5895-312-30-C1-51

Receiver relay card 1522307, schematic diagram.

761-494 O - 65 - Fols. Text No. 25



USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
DIODE	CR1	NONE
RELAY	K4	NONE
SWITCH	S1	NONE

2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.

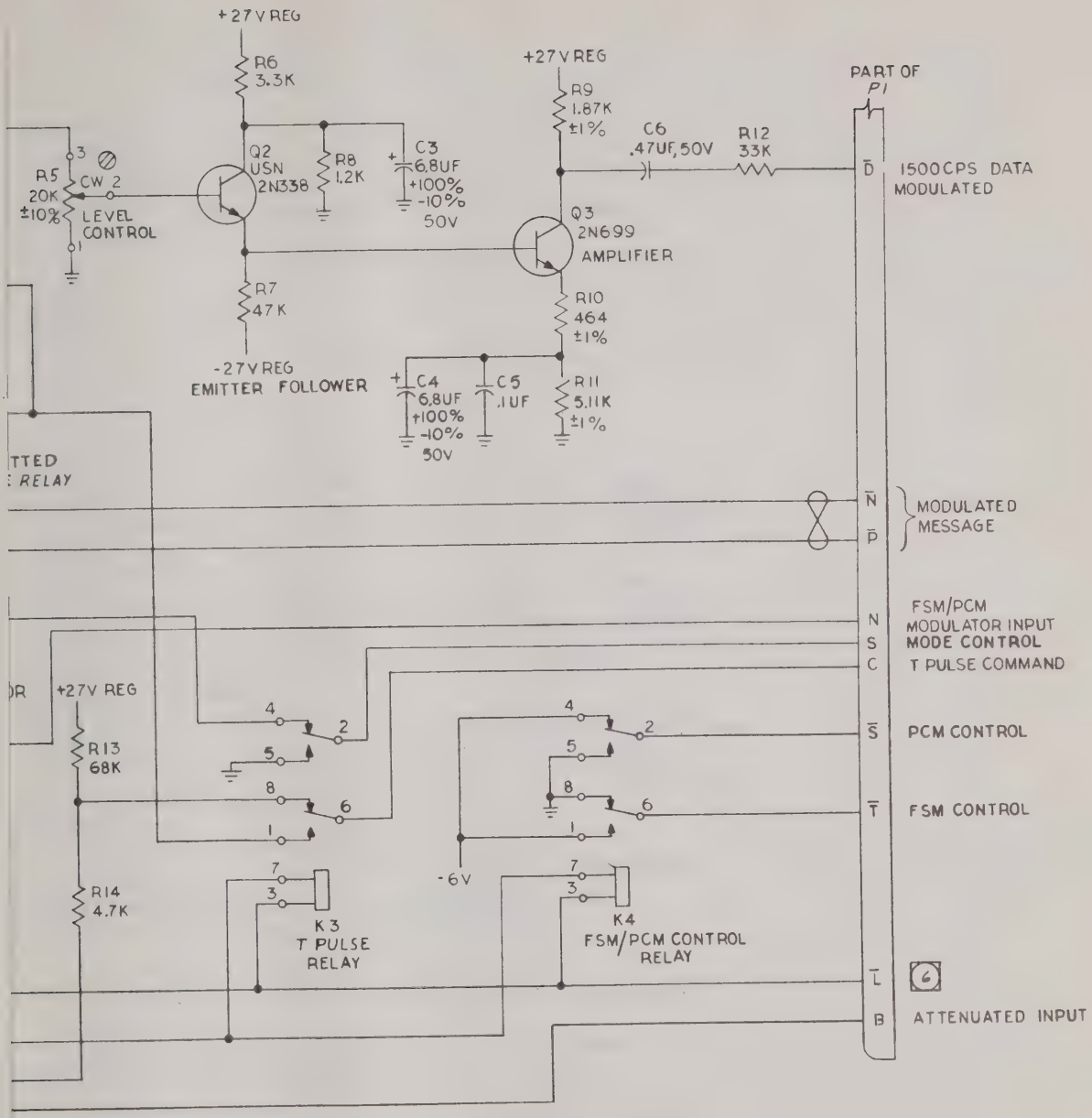
1. FOR ASSEMBLY SEE DRAWING NO. 1522307

NOTES: UNLESS OTHERWISE SPECIFIED

TM5895-312-30-C1-51

Figure 30. Receiver relay card 1522307, schematic diagram.

761-494 O - 65 - Pols. Text No. 25



6 FOR SIGNAL INFO SEE UNIT SCHEMATIC.

5. RELAYS SHOWN IN DE-ENERGIZED FSM POSITION.

4. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NO. OR ASSEMBLY DESIGNATION OR BOTH.

3. CAPACITANCE VALUES ARE IN MICROFARADS ±10%, 100V. TOLERANCE AND WATTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.

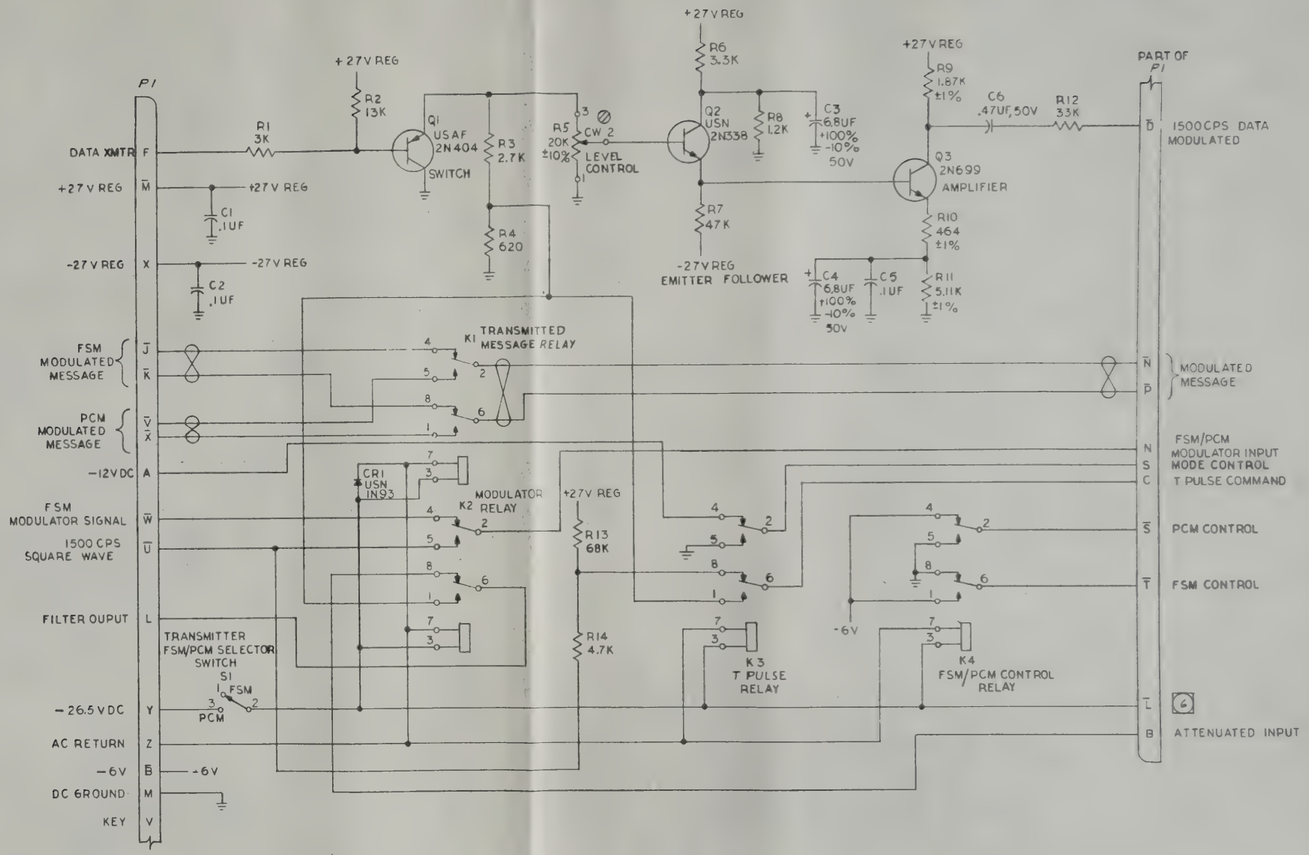
2. RESISTANCE VALUES ARE IN OHMS ±5%, 1/2 WATT. TOLERANCE AND WATTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.

1. FOR ASSEMBLY SEE DRAWING NO. 1522312.

NOTES: UNLESS OTHER WISE SPECIFIED

TM 5895-312-30-52

mplifier and transmitter relay card 1522312, schematic diagram.



USED ON THIS DRAWING		
COMPONENT	HIGHEST NUMBER	NUMBERS NOT USED
CAPACITOR	C6	NONE
RESISTOR	R14	NONE
TRANSISTOR	Q3	NONE
DIODE	CR1	NONE
RELAY	K4	NONE
SWITCH	S1	NONE

6 FOR SIGNAL INFO SEE UNIT SCHEMATIC.

5. RELAYS SHOWN IN DE-ENERGIZED FSM POSITION.

4. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NO. OR ASSEMBLY DESIGNATION OR BOTH.

3. CAPACITANCE VALUES ARE IN MICROFARADS ±10% 300V. TOLERANCE AND WATTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.

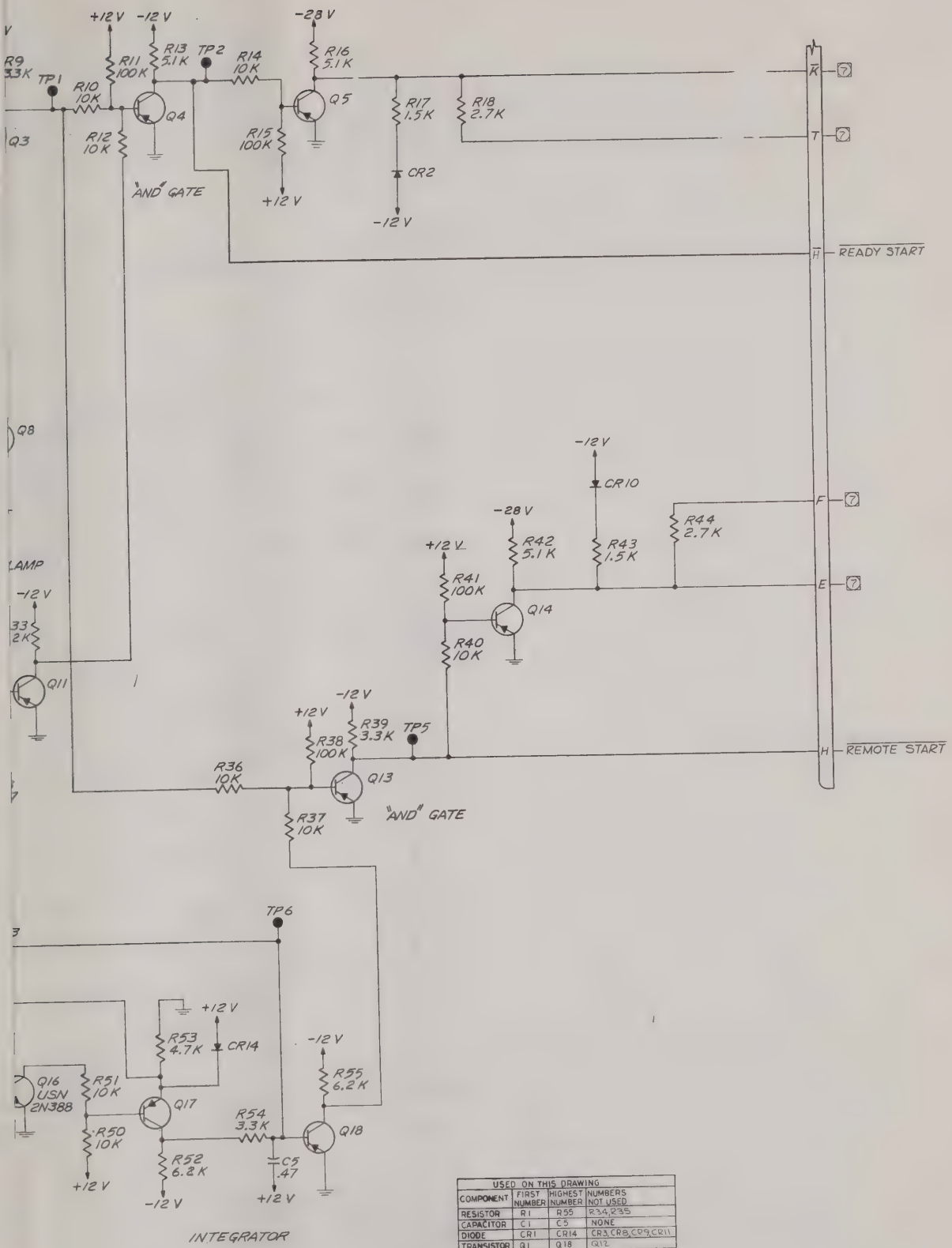
2. RESISTANCE VALUES ARE IN OHMS ±5%, 1/2 WATT. TOLERANCE AND WATTAGE DESIGNATED REPRESENT MINIMUM REQUIREMENTS.

1. FOR ASSEMBLY SEE DRAWING NO. 1522312.

NOTES: UNLESS OTHER WISE SPECIFIED

TM 5695-312-30-52

Figure 31. Variable gain amplifier and transmitter relay card 1522312, schematic diagram.

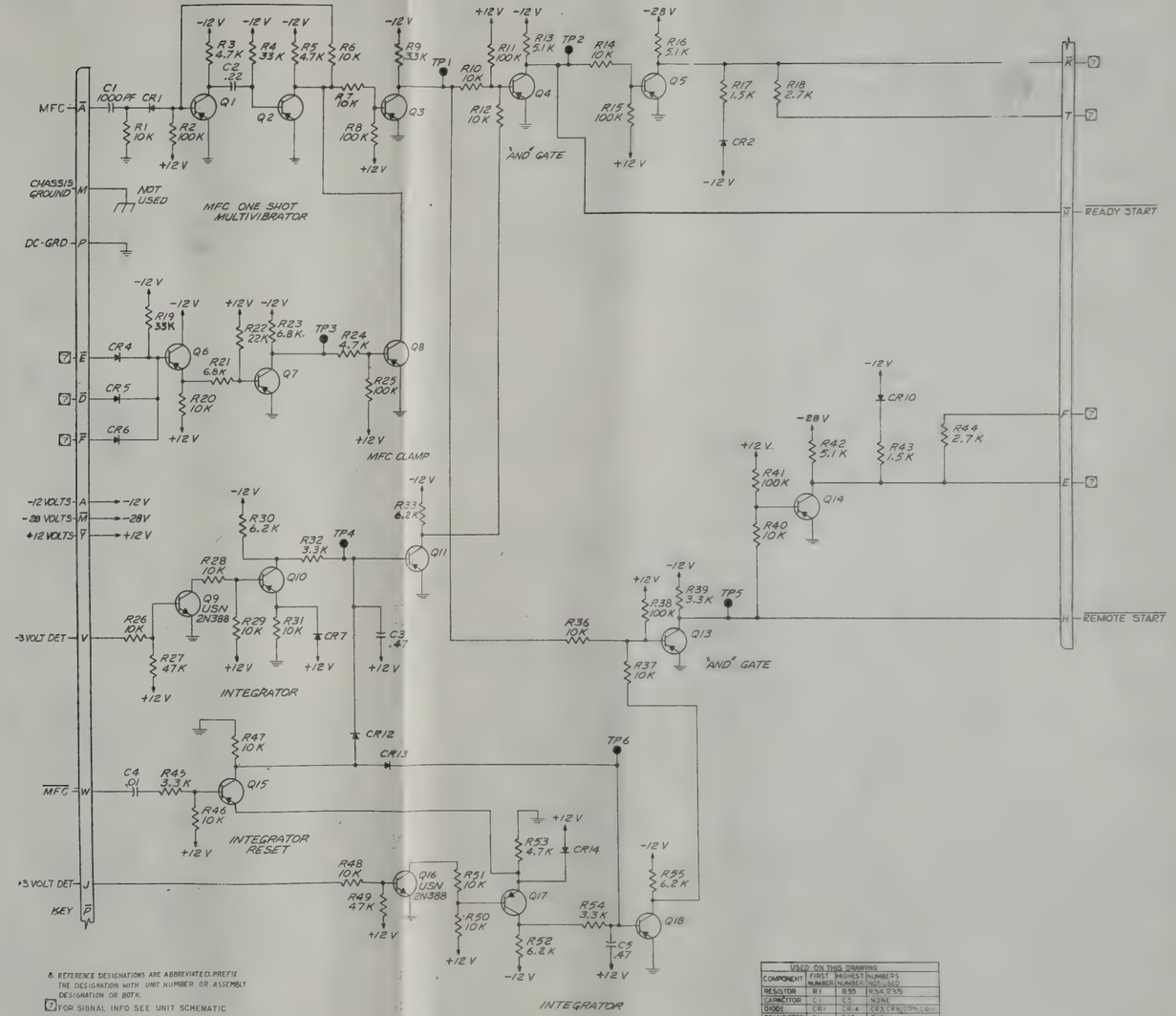


USED ON THIS DRAWING			
COMPONENT	FIRST NUMBER	HIGHEST NUMBER	NUMBERS NOT USED
RESISTOR	R1	R55	R34, R35
CAPACITOR	C1	C5	NONE
DIODE	CR1	CR14	CR3, CR8, CR9, CR11
TRANSISTOR	Q1	Q18	Q12

TM5895-312-30-C1-53

ure 32. Detector start/remote 1522348, schematic diagram.

761-494 O - 65 - Fols. Text No. 27



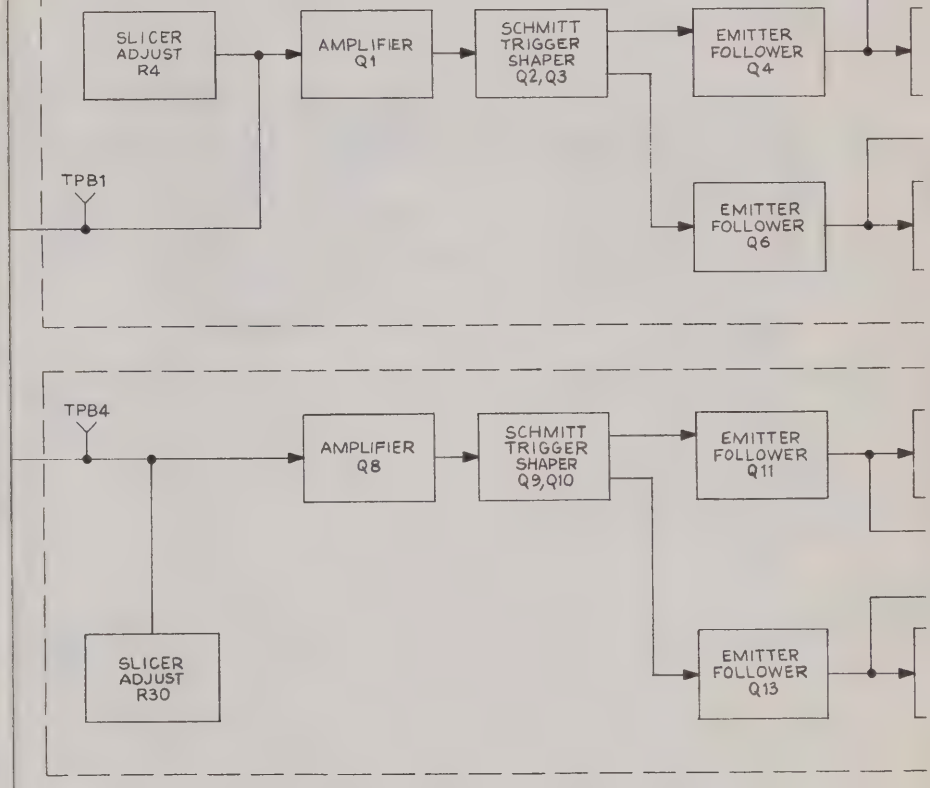
USED ON THIS DRAWING			
COMPONENT	FIRST NUMBER	HIGHEST NUMBER	NUMBERS NOT USED
RESISTOR	R1	R55	R54,R35
CAPACITOR	C1	C5	NONE
DIODE	CR1	CR14	CR3,CR8,CR9,CR11
TRANSISTOR	Q1	Q18	Q12

NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR ASSY SEE DWG NO. 1522348
2. RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT
3. CAPACITANCE VALUES ARE IN MICROFARADS ±10%, 50 V
4. DIODES ARE JAN1N276
5. TRANSISTORS ARE USAF 2N404
6. TP = TEST POINT
7. FOR SIGNAL INFO SEE UNIT SCHEMATIC
8. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.

TM5895-312-30-C1-53

Figure 32. Detector start/remote 1522348, schematic diagram.

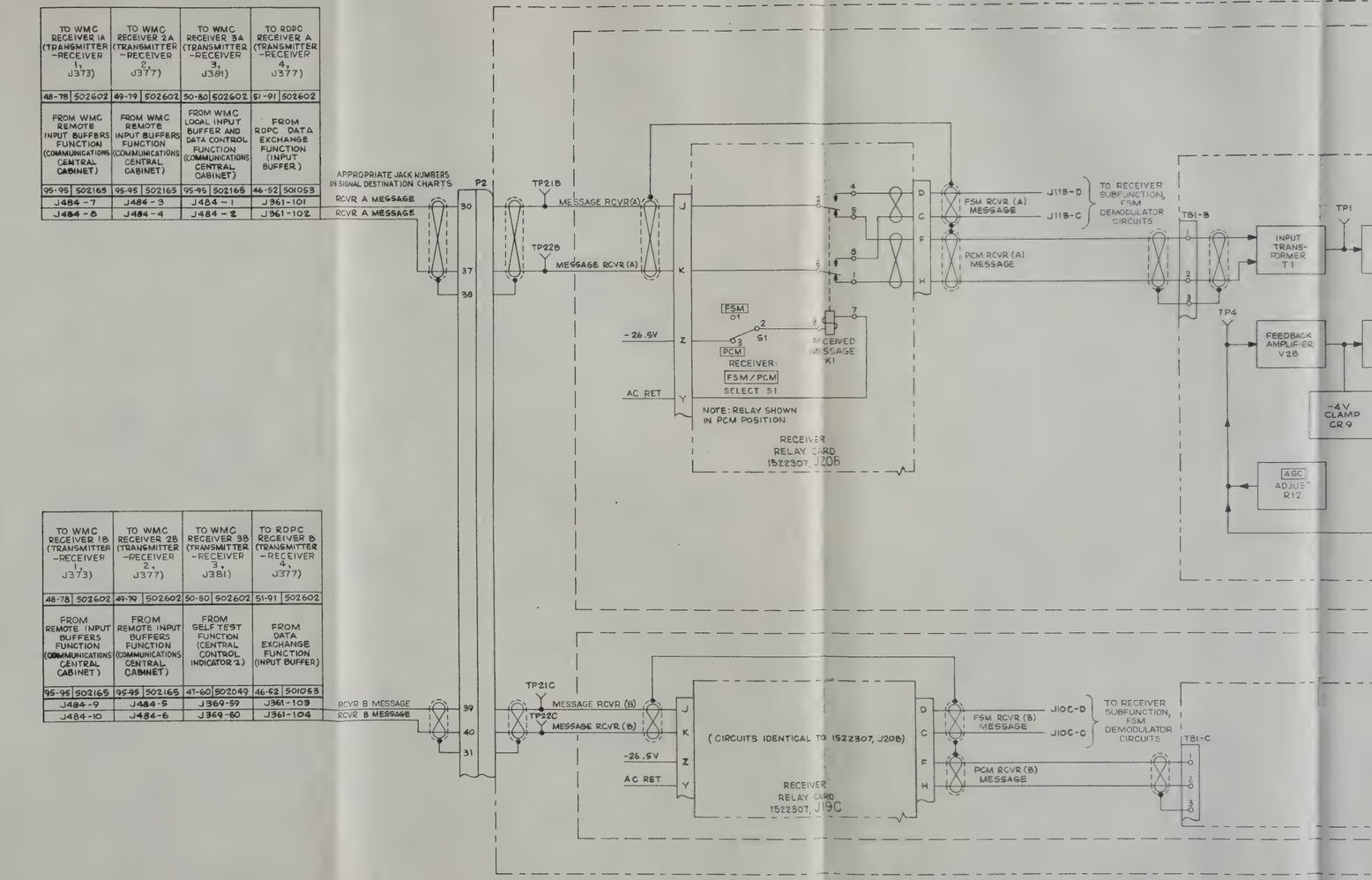


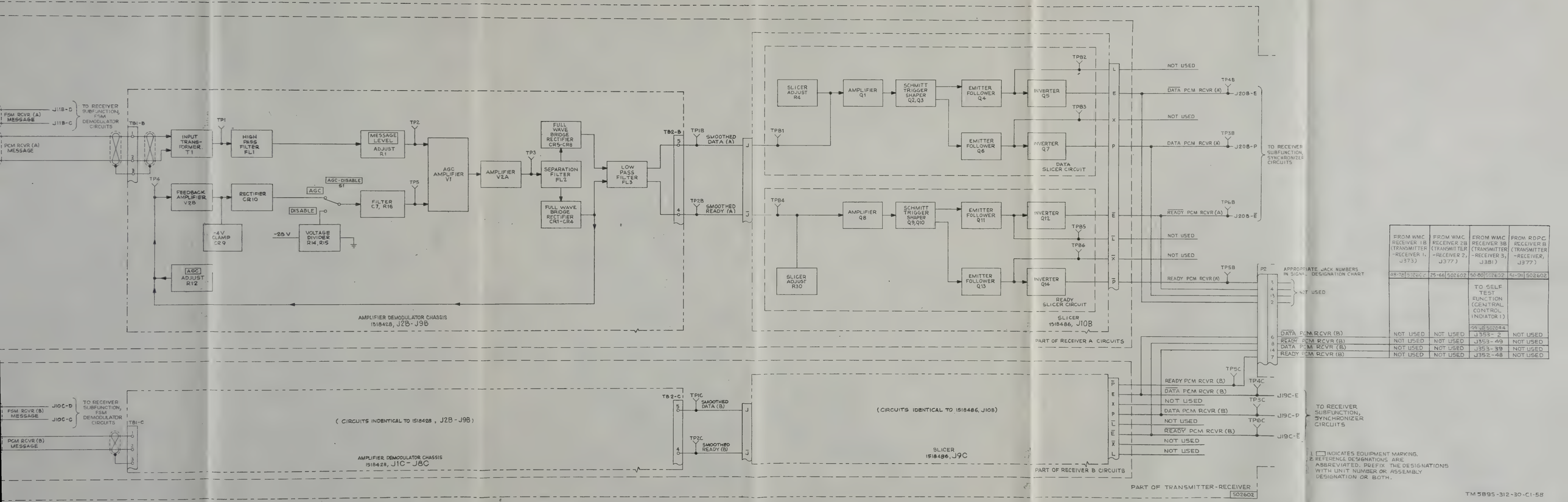
(CIRCUITS IDENTICAL TO 1518486, J10B)

SLICER
1518486, J9C

TO WMC RECEIVER 1A (TRANSMITTER-RECEIVER 1, J373)	TO WMC RECEIVER 2A (TRANSMITTER-RECEIVER 2, J377)	TO WMC RECEIVER 3A (TRANSMITTER-RECEIVER 3, J381)	TO RDPC RECEIVER A (TRANSMITTER-RECEIVER 4, J377)
48-78 | 502602	49-79 | 502602	50-80 | 502602	51-91 | 502602
FROM WMC REMOTE INPUT BUFFERS FUNCTION (COMMUNICATIONS CENTRAL CABINET)	FROM WMC REMOTE INPUT BUFFERS FUNCTION (COMMUNICATIONS CENTRAL CABINET)	FROM WMC LOCAL INPUT BUFFER AND DATA CONTROL FUNCTION (COMMUNICATIONS CENTRAL CABINET)	FROM RDPC DATA EXCHANGE FUNCTION (INPUT BUFFER)
95-95 | 502165	95-95 | 502165	95-95 | 502166	46-52 | 501053
J484-7	J484-3	J484-1	J361-101
J484-8	J484-4	J484-2	J361-102

TO WMC RECEIVER 1B (TRANSMITTER-RECEIVER 1, J373)	TO WMC RECEIVER 2B (TRANSMITTER-RECEIVER 2, J377)	TO WMC RECEIVER 3B (TRANSMITTER-RECEIVER 3, J381)	TO RDPC RECEIVER B (TRANSMITTER-RECEIVER 4, J377)
48-78 | 502602	49-79 | 502602	50-80 | 502602	51-91 | 502602
FROM REMOTE INPUT BUFFERS FUNCTION (COMMUNICATIONS CENTRAL CABINET)	FROM REMOTE INPUT BUFFERS FUNCTION (COMMUNICATIONS CENTRAL CABINET)	FROM SELF TEST FUNCTION (CENTRAL CONTROL INDICATOR 2)	FROM DATA EXCHANGE FUNCTION (INPUT BUFFER)
95-95 | 502165	95-95 | 502165	47-60 | 502049	46-52 | 501053
J484-9	J484-5	J369-59	J361-103
J484-10	J484-6	J369-60	J361-104



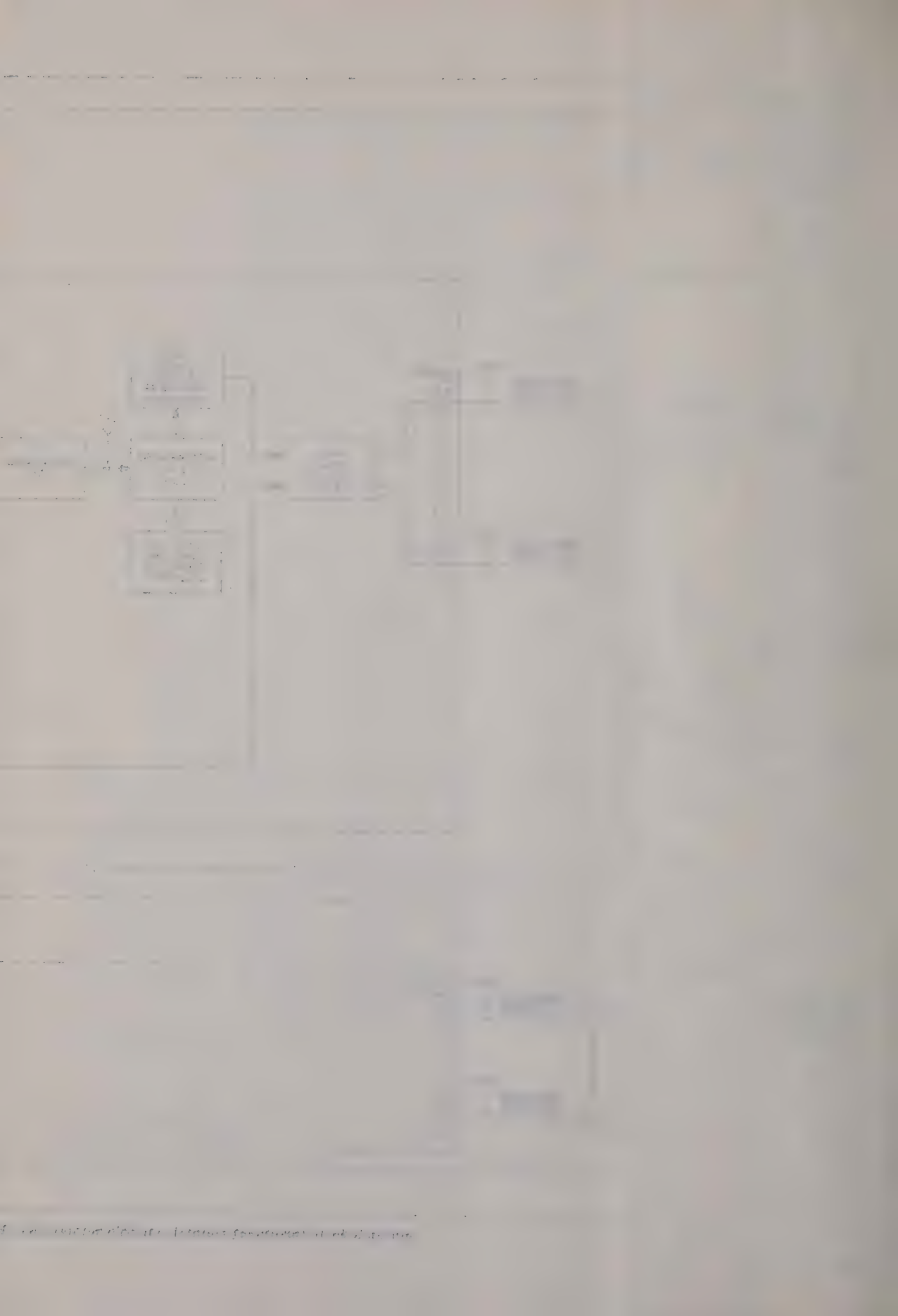


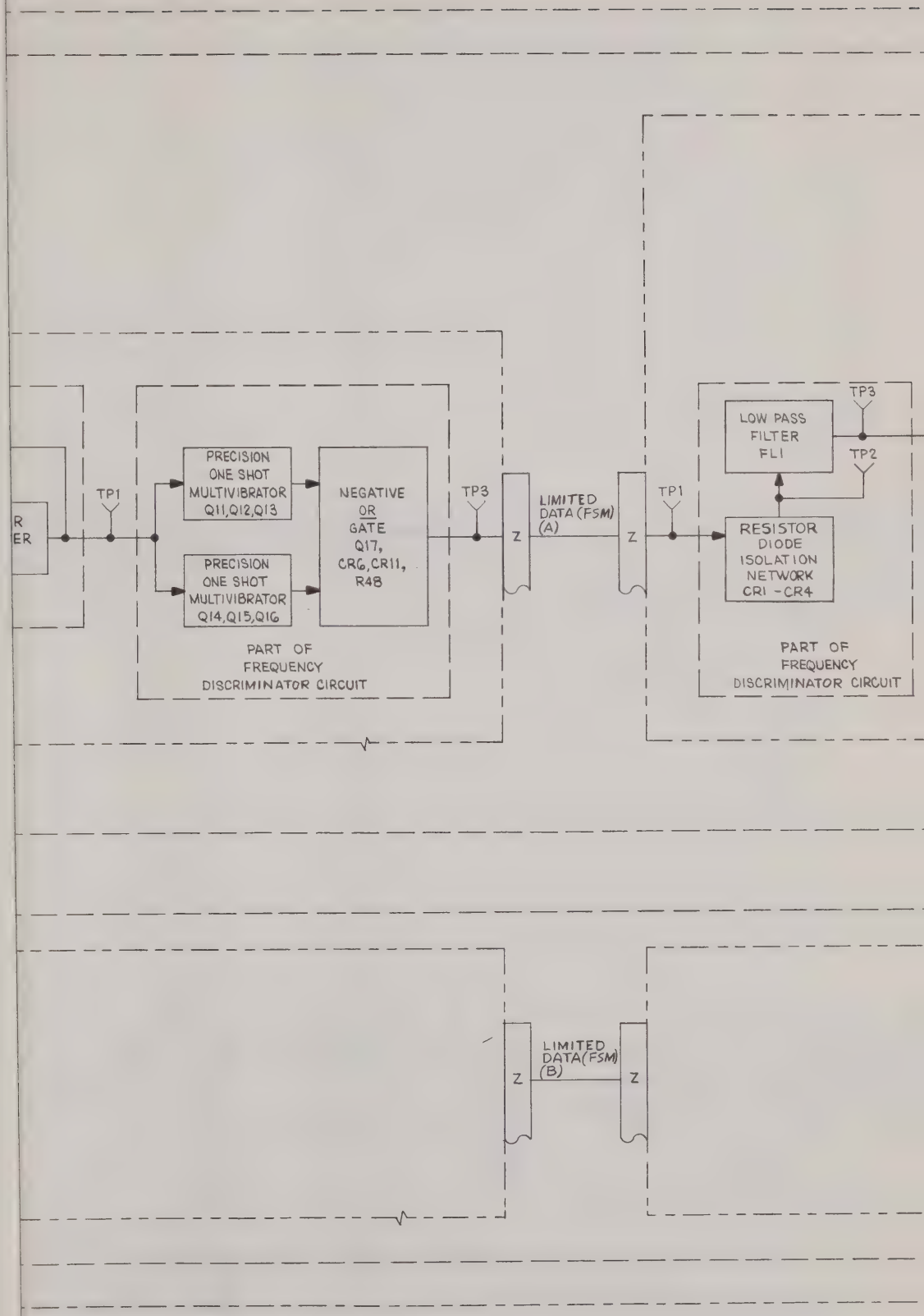
APPROPRIATE JACK NUMBERS IN SIGNAL DESIGNATION CHART	FROM WMC RECEIVER 1B (TRANSMITTER -RECEIVER 1, J373)	FROM WMC RECEIVER 2B (TRANSMITTER -RECEIVER 2, J377)	FROM WMC RECEIVER 3B (TRANSMITTER -RECEIVER 3, J381)	FROM RDPC RECEIVER B (TRANSMITTER -RECEIVER, J377)
	48-78 502602	25-66 502602	50-80 502602	51-91 502602
NOT USED			TO SELF TEST FUNCTION (CENTRAL CONTROL INDIATOR 1) 99 of 502044	
DATA PCM RCVR (B)	NOT USED	NOT USED	J353- 2	NOT USED
READY PCM RCVR (B)	NOT USED	NOT USED	J353- 49	NOT USED
DATA PCM RCVR (B)	NOT USED	NOT USED	J353- 39	NOT USED
READY PCM RCVR (B)	NOT USED	NOT USED	J352- 48	NOT USED

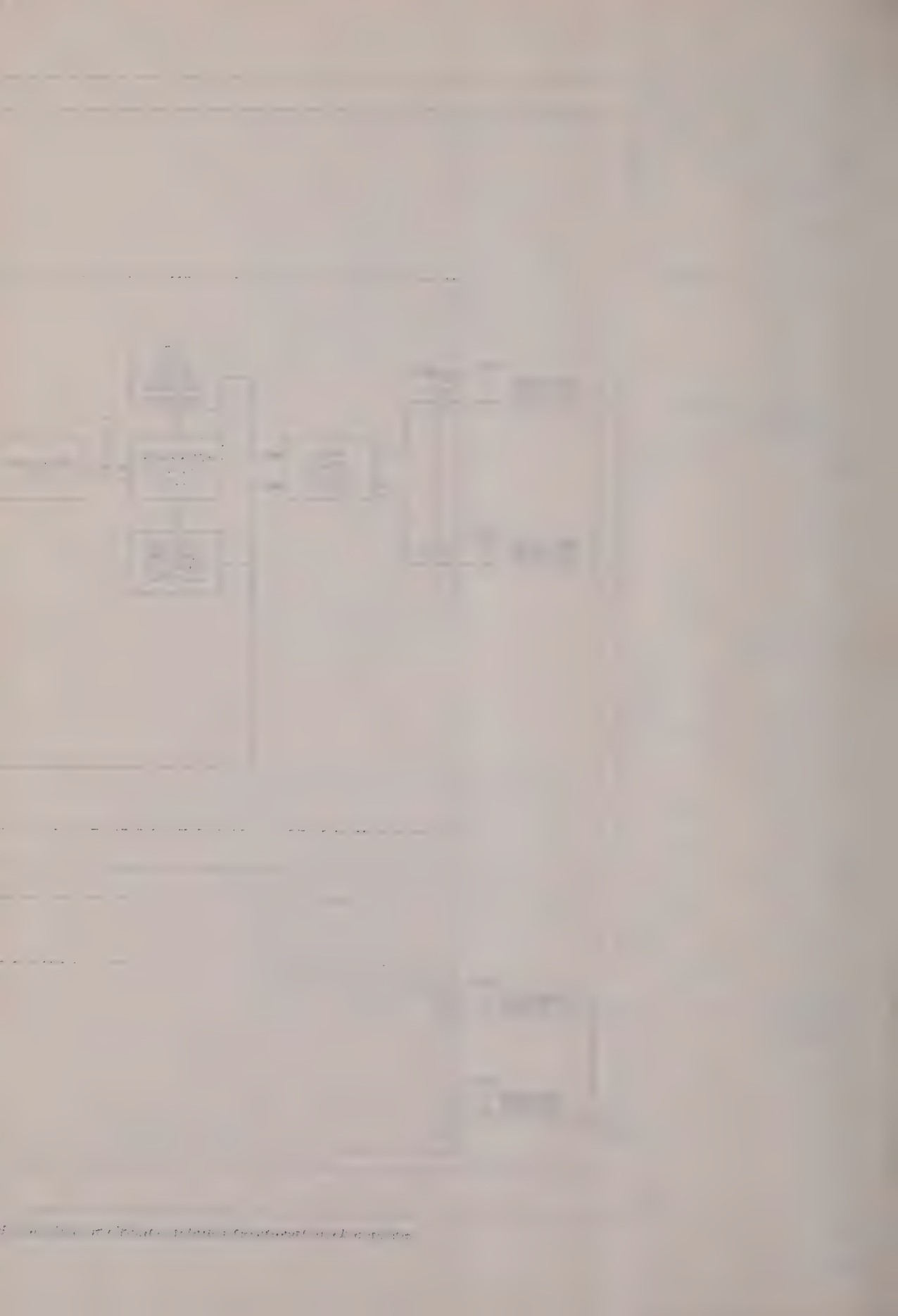
1. ☐ INDICATES EQUIPMENT MARKING.
2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.

TM 5895-312-30-C1-58

Figure 37. Receiver subfunction PCM demodulator circuits, detailed functional block diagram.




R
ER
TP1
PRECISION
ONE SHOT
MULTIVIBRATOR
Q11,Q12,Q13
PRECISION
ONE SHOT
MULTIVIBRATOR
Q14,Q15,Q16
NEGATIVE
OR
GATE
Q17,
CR6,CR11,
R48
PART OF
FREQUENCY
DISCRIMINATOR CIRCUIT
TP3
Z
LIMITED
DATA (FSM)
(A)
Z
TP1
LOW PASS
FILTER
FL1
TP3
TP2
RESISTOR
DIODE
ISOLATION
NETWORK
CR1 - CR4
PART OF
FREQUENCY
DISCRIMINATOR CIRCUIT
Z
LIMITED
DATA(FSM)
(B)
Z



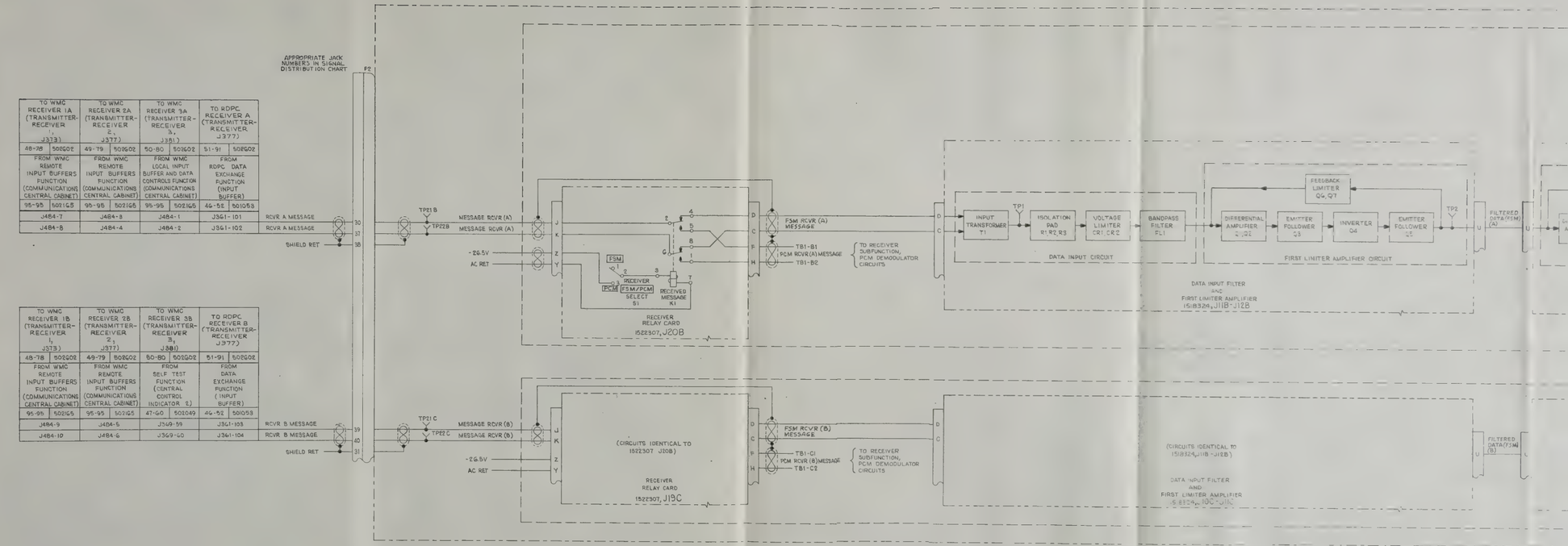


Figure 38①. Receiver subfunction FSM demodulator circuits, d

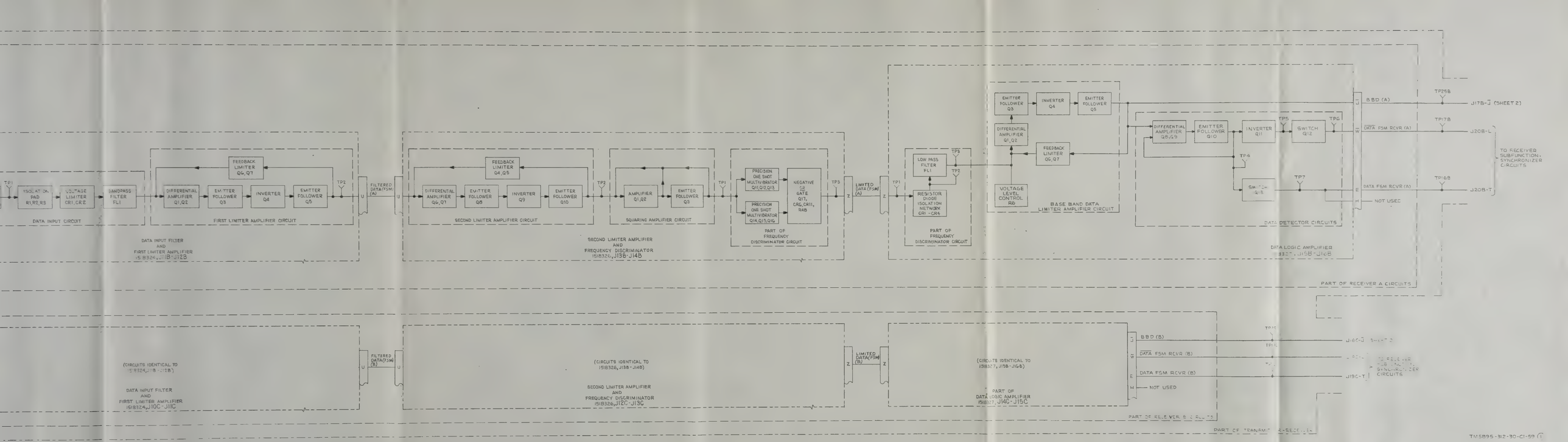
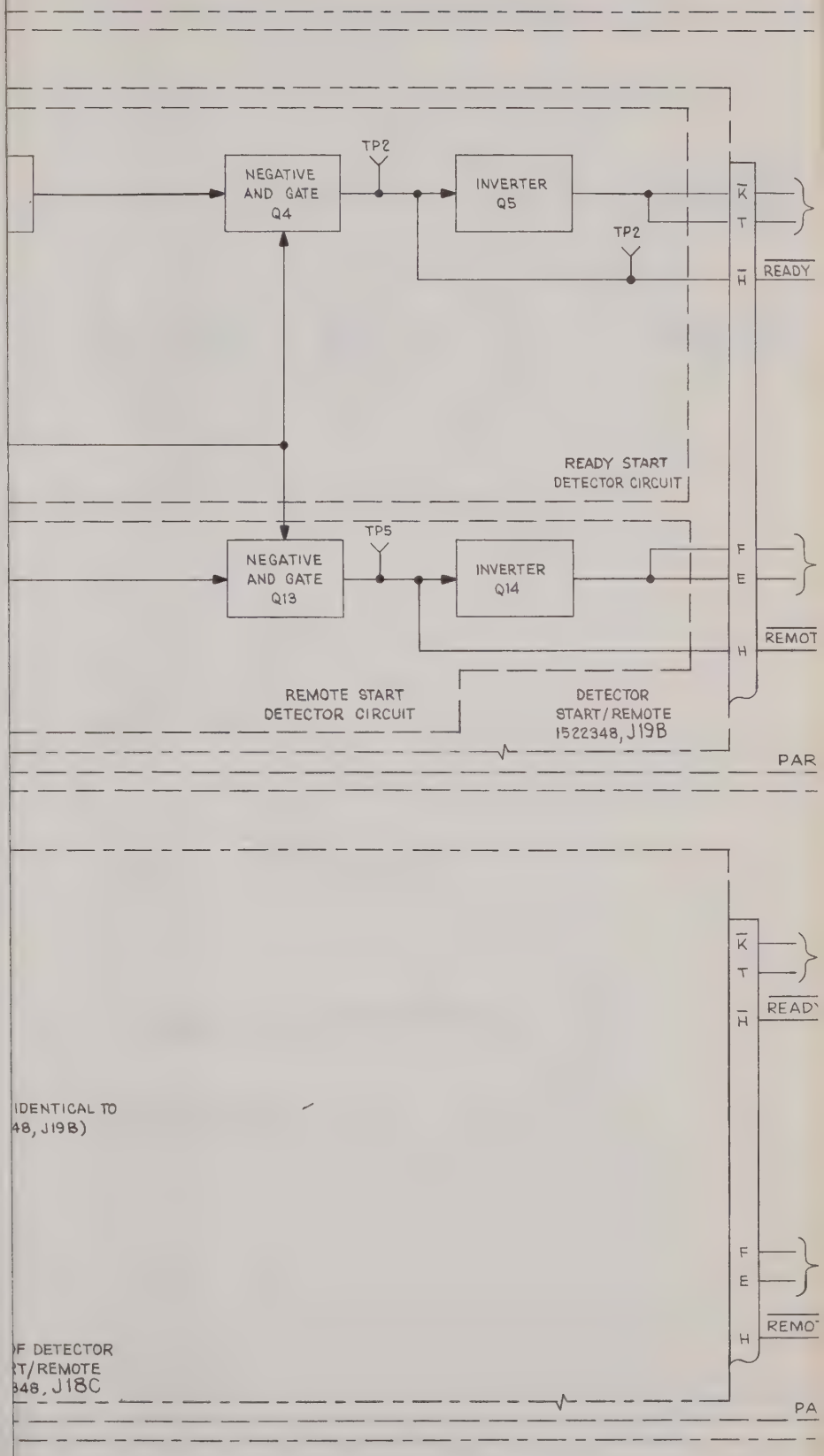


Figure 38(). Receiver subfunction FSM demodulator circuits, detailed functional block diagram (part 1 of 2).

TM5895-312-30-C1-59 (1)


NEGATIVE AND GATE Q4
TP2
INVERTER Q5
TP2
READY
READY START DETECTOR CIRCUIT
NEGATIVE AND GATE Q13
TP5
INVERTER Q14
REMOT
REMOTE START DETECTOR CIRCUIT
DETECTOR START/REMOTE 1522348, J19B
PAR
IDENTICAL TO
48, J19B)
F DETECTOR
RT/REMOTE
348, J18C
READ
REMO
PA

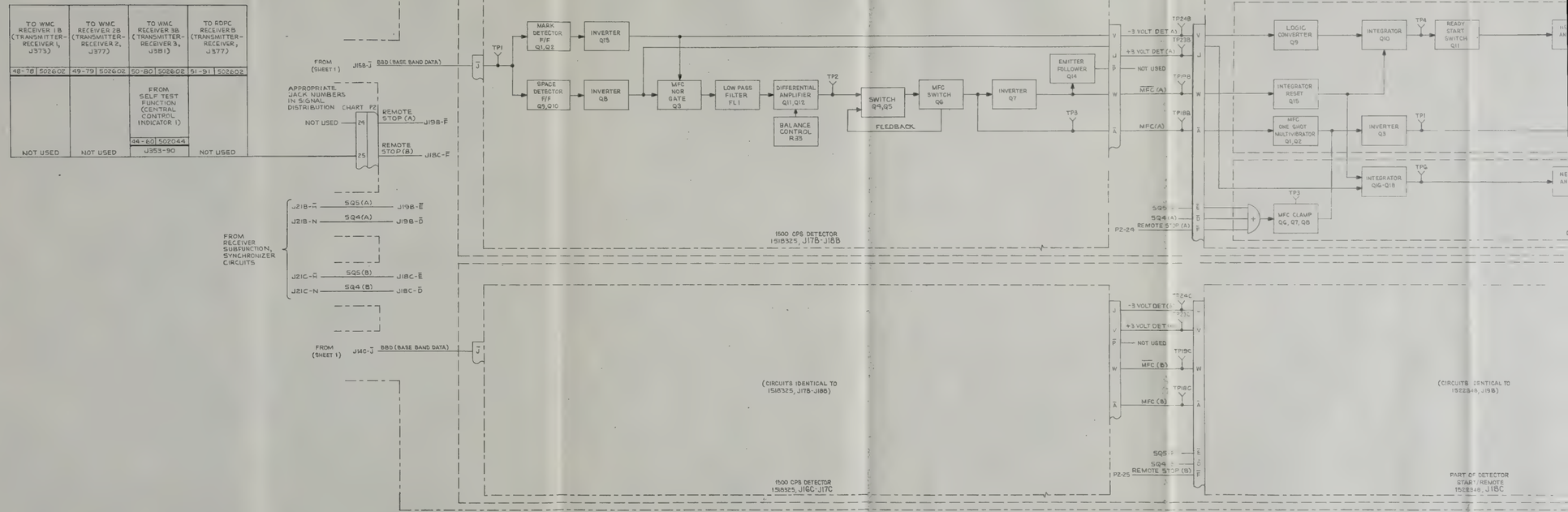


Figure 38①. Receiver subfunction FSM demodulator circuits, detailed functional block diagram (part 2 of 2).

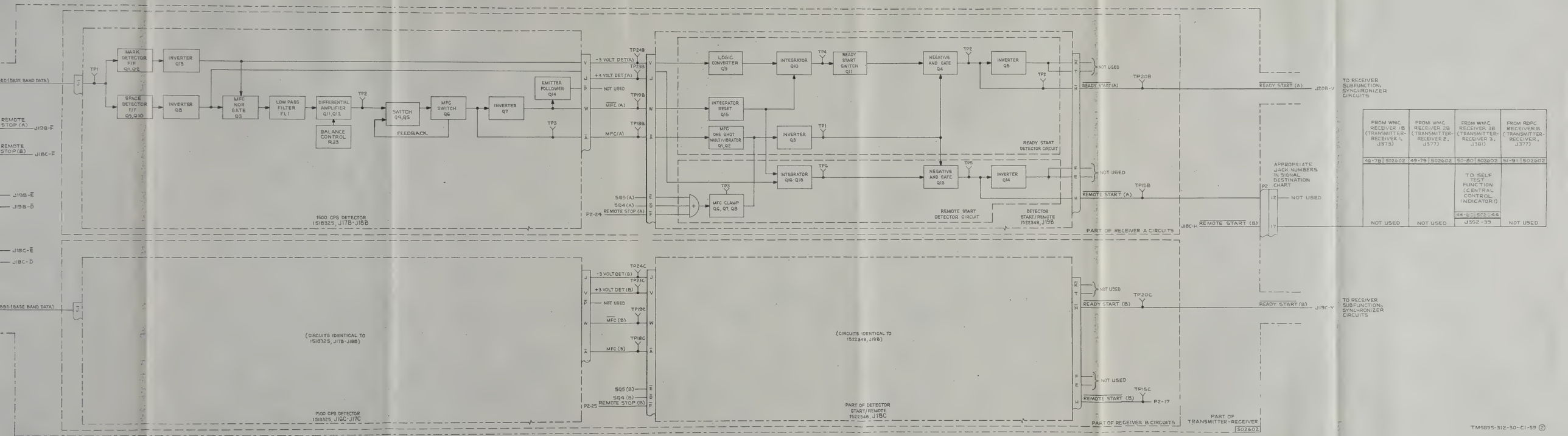
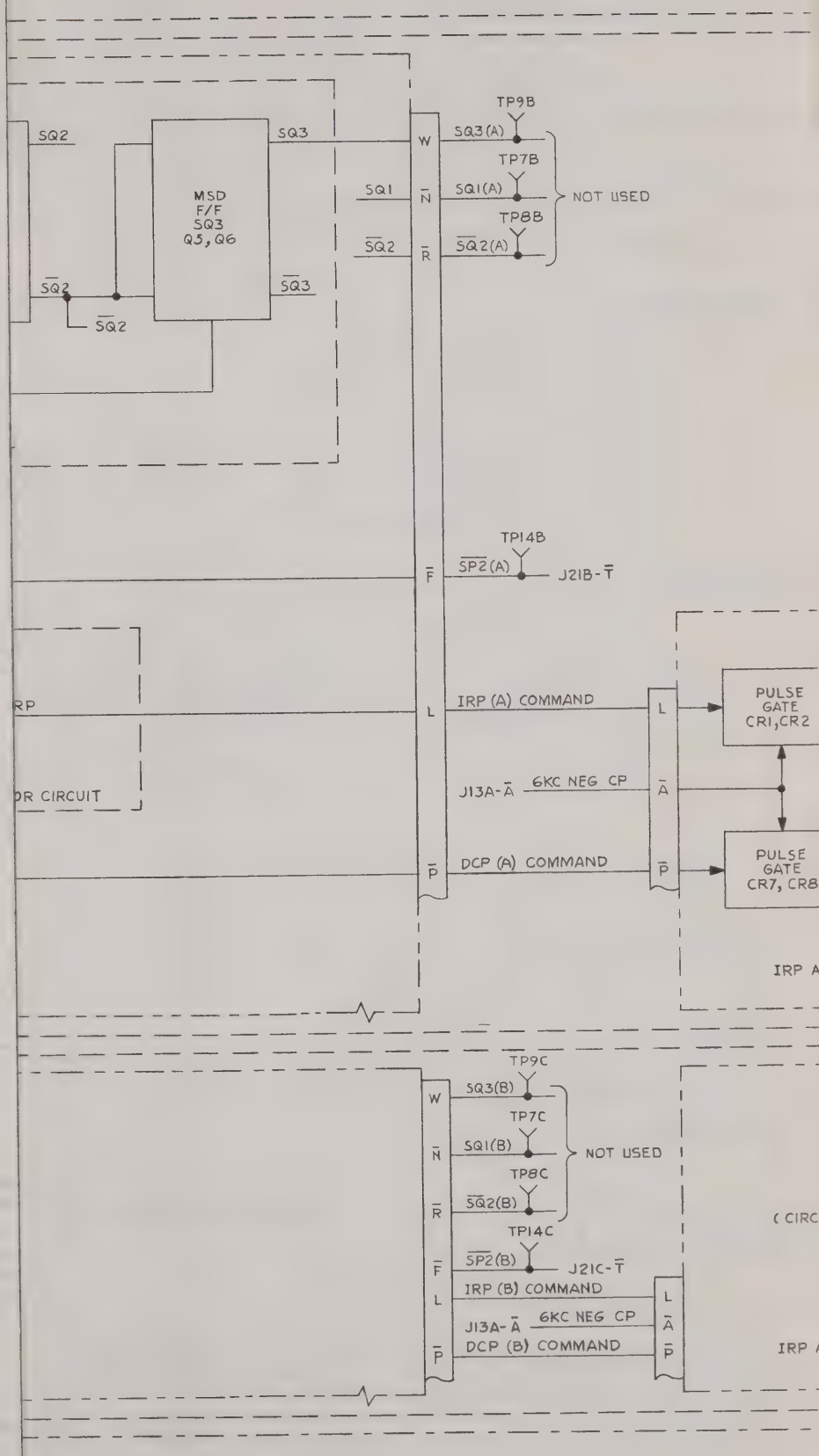


Figure 38(2). Receiver subfunction FSM demodulator circuits, detailed functional block diagram (part 2 of 2).



761-494 O - 65 - Fols. Text No. 31

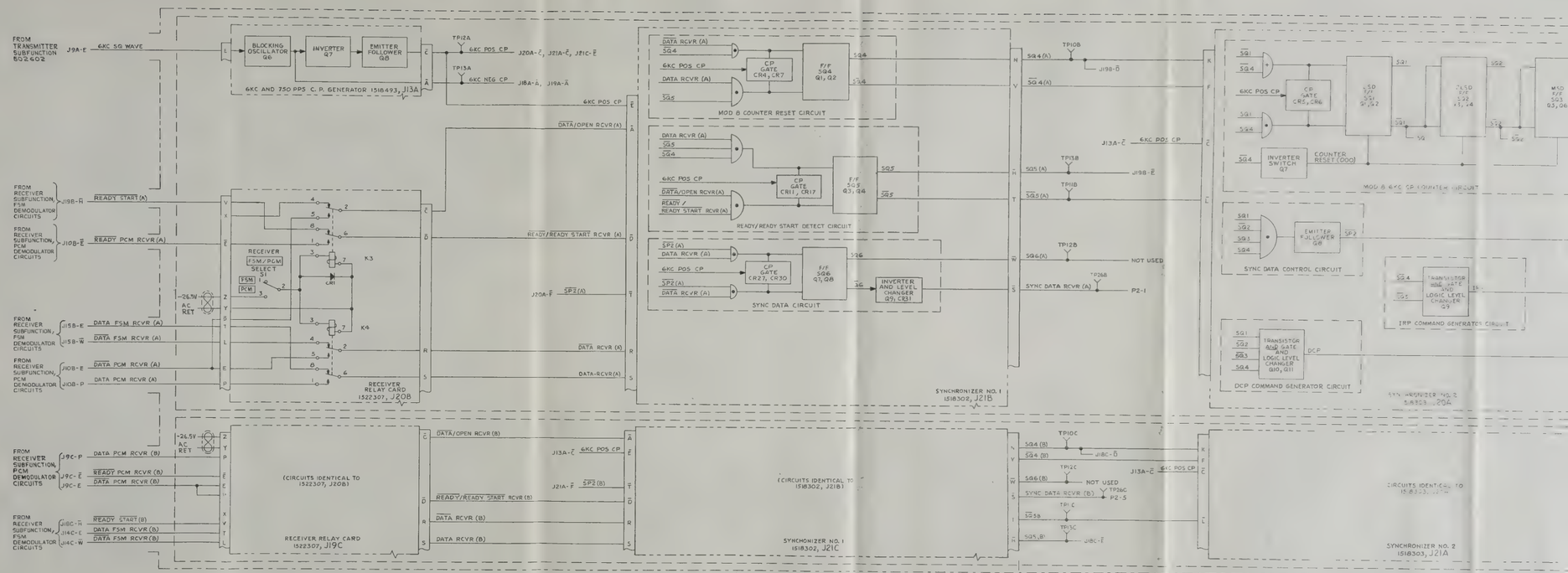


Figure 39. Receiver subfunction, synchronizer circuits, detailed functional block diagram.

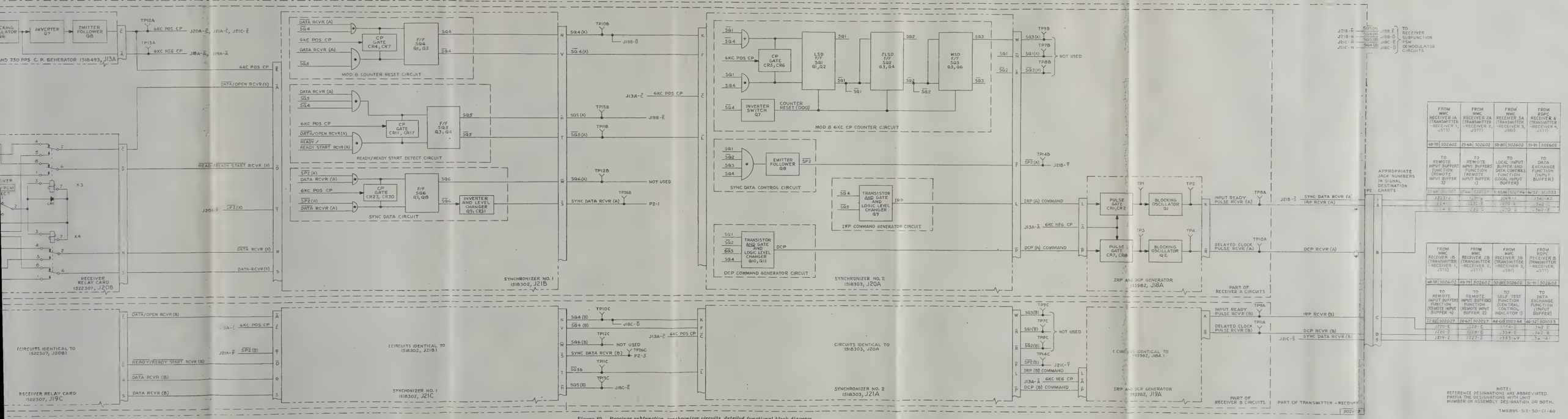
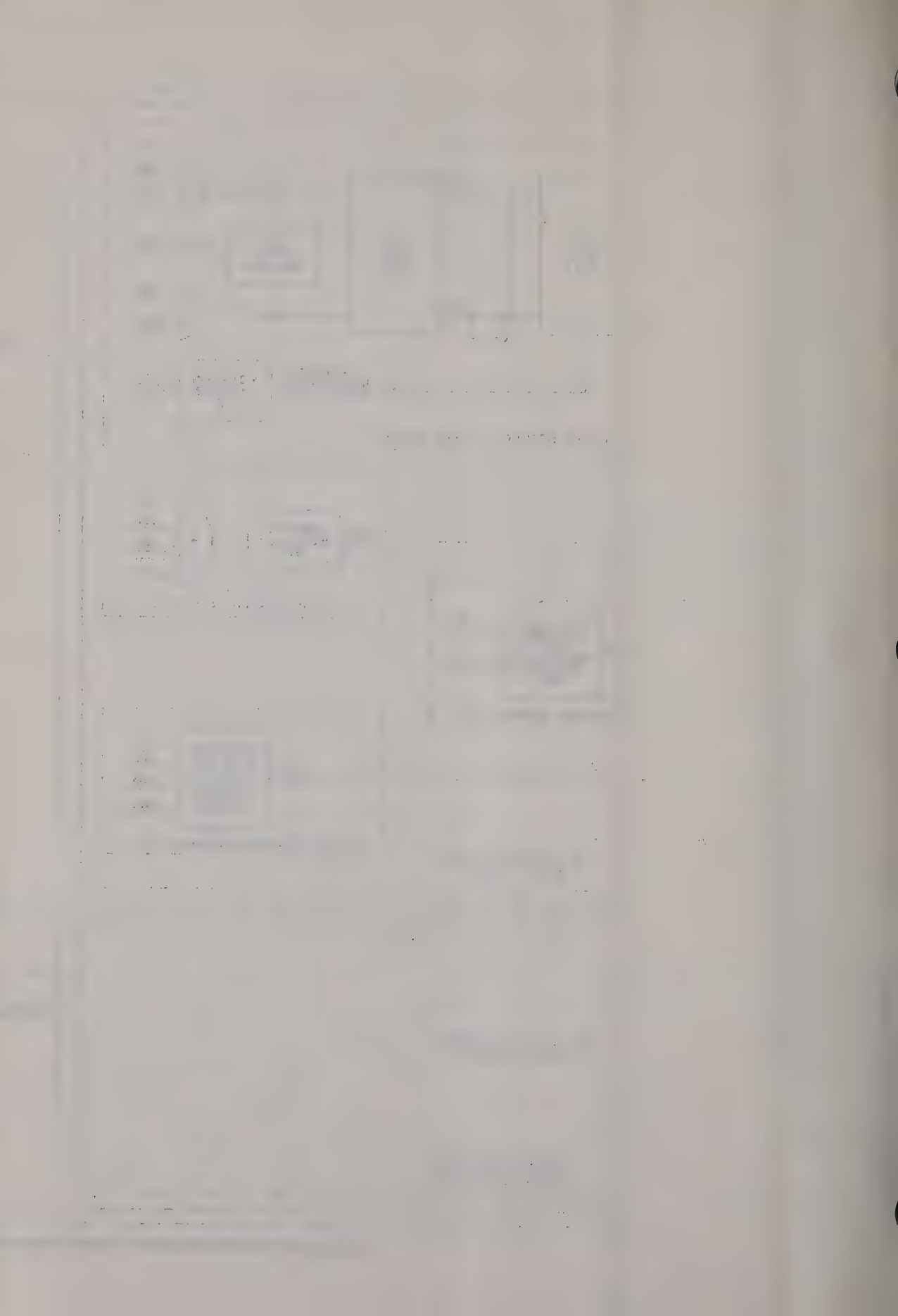
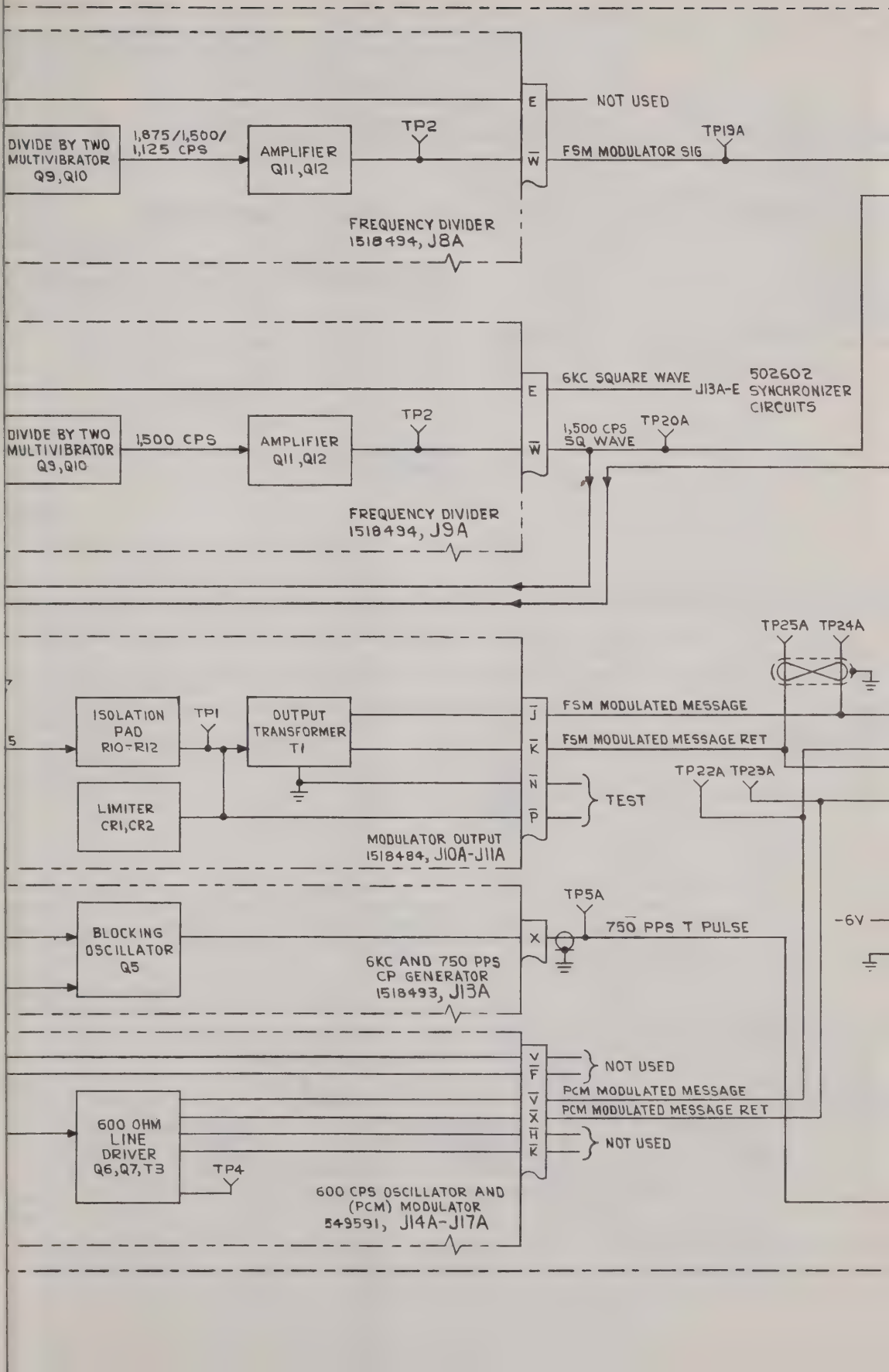


Figure 39. Receiver subfunction, synchronizer circuits, detailed functional block diagram.




DIVIDE BY TWO MULTIVIBRATOR Q9, Q10
1,875/1,500/ 1,125 CPS
AMPLIFIER Q11, Q12
TP2
E
W
NOT USED
TP19A
FSM MODULATOR SIG
FREQUENCY DIVIDER 1518494, J8A
DIVIDE BY TWO MULTIVIBRATOR Q9, Q10
1,500 CPS
AMPLIFIER Q11, Q12
TP2
E
W
6KC SQUARE WAVE
J13A-E
502602 SYNCHRONIZER CIRCUITS
1,500 CPS SQ WAVE
TP20A
FREQUENCY DIVIDER 1518494, J9A
TP25A
TP24A
ISOLATION PAD R10-R12
TP1
OUTPUT TRANSFORMER T1
LIMITER CR1, CR2
J
K
N
P
FSM MODULATED MESSAGE
FSM MODULATED MESSAGE RET
TEST
TP22A
TP23A
MODULATOR OUTPUT 1518484, J10A-J11A
BLOCKING OSCILLATOR Q5
TP5A
X
750 PPS T PULSE
-6V
6KC AND 750 PPS CP GENERATOR 1518493, J13A
V
F
NOT USED
PCM MODULATED MESSAGE
PCM MODULATED MESSAGE RET
NOT USED
600 OHM LINE DRIVER Q6, Q7, T3
TP4
600 CPS OSCILLATOR AND (PCM) MODULATOR 549591, J14A-J17A

TO WMC TRANSMITTER 1 (TRANSMITTER-RECEIVER 1 J373)	TO WMC TRANSMITTER 2 (TRANSMITTER-RECEIVER 2 J377)	TO WMC TRANSMITTER 3 (TRANSMITTER-RECEIVER 3 J381)	TO RDPC TRANSMITTER (TRANSMITTER-RECEIVER J377)
48-78 | 502602	49-79 | 502602	50-80 | 502602	51-81 | 502602
FROM REMOTE OUTPUT BUFFER FUNCTION (COMMUNICATIONS CENTRAL CABINET)	FROM LOCAL OUTPUT BUFFER FUNCTION (COMMUNICATIONS CENTRAL CABINET)	FROM SELF TEST FUNCTION (COMMUNICATIONS CENTRAL CABINET)	FROM DATA EXCHANGE FUNCTION (OUTPUT BUFFER)
95-95 | 502165	95-95 | 502165	95-95 | 502165	47-56 | 501054
J484-43	J484-48	J484-38	J364-60
J484-42	J484-49	J484-37	J364-61

(APPROPRIATE JACK NUMBERS IN SIGNAL DESTINATION CHART)

P2

DATA CONTROL — 29

READY CONTROL — 32

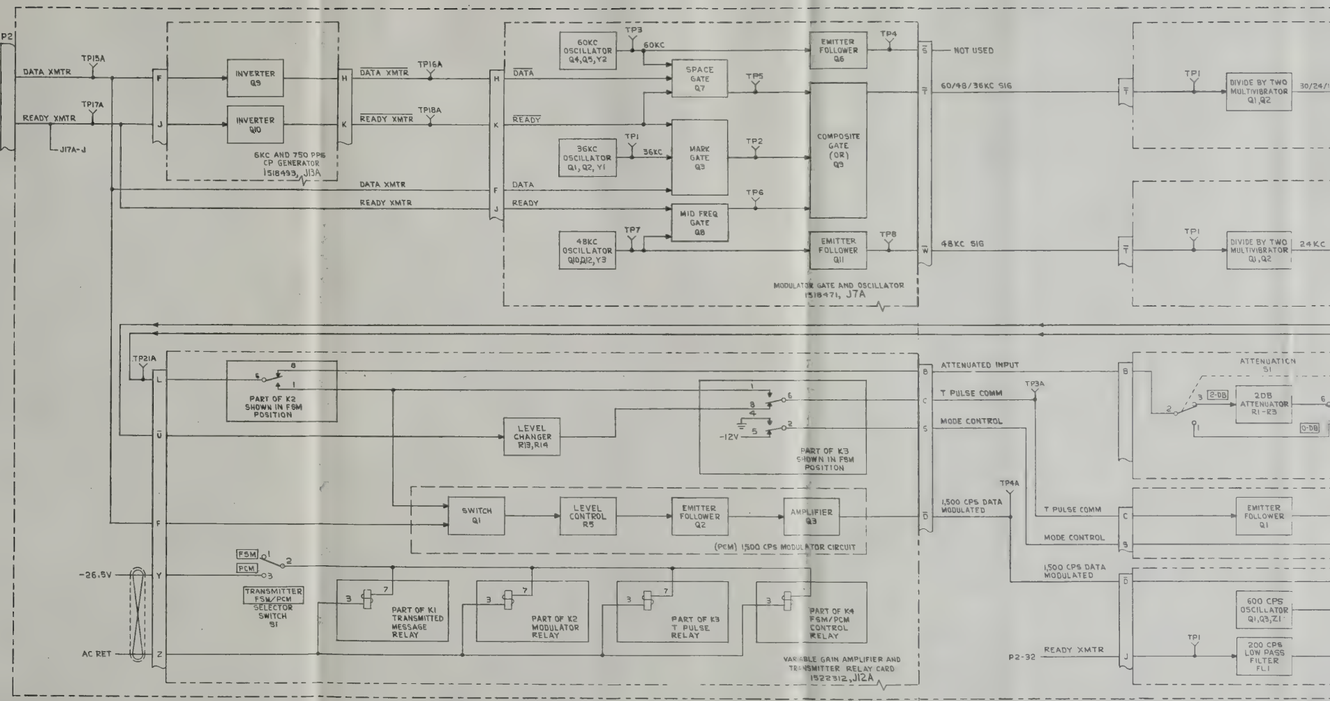


Figure 40. Transmitter

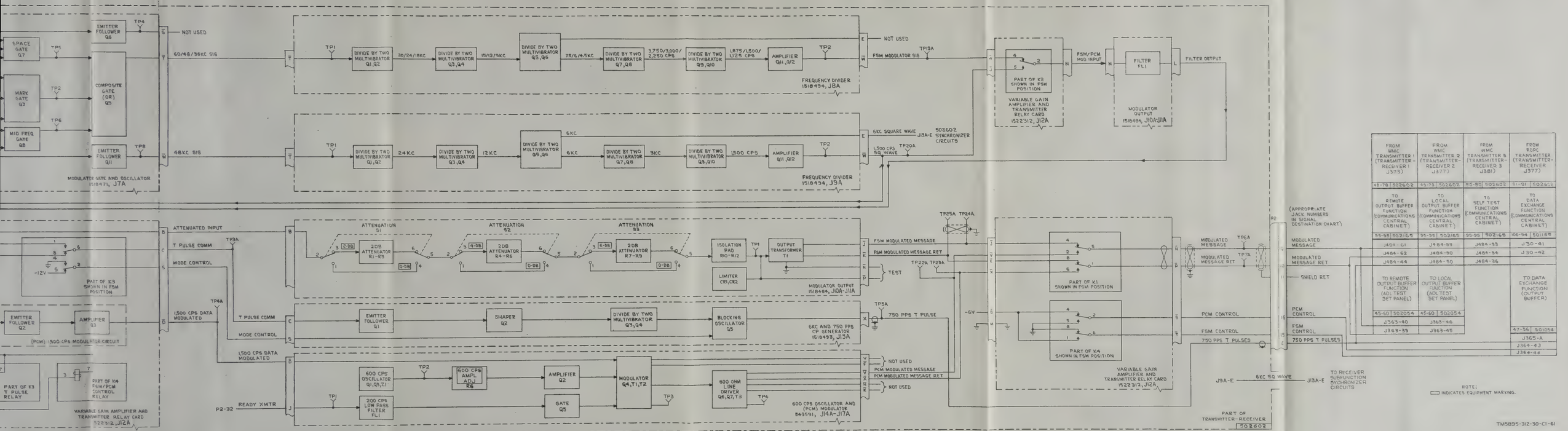
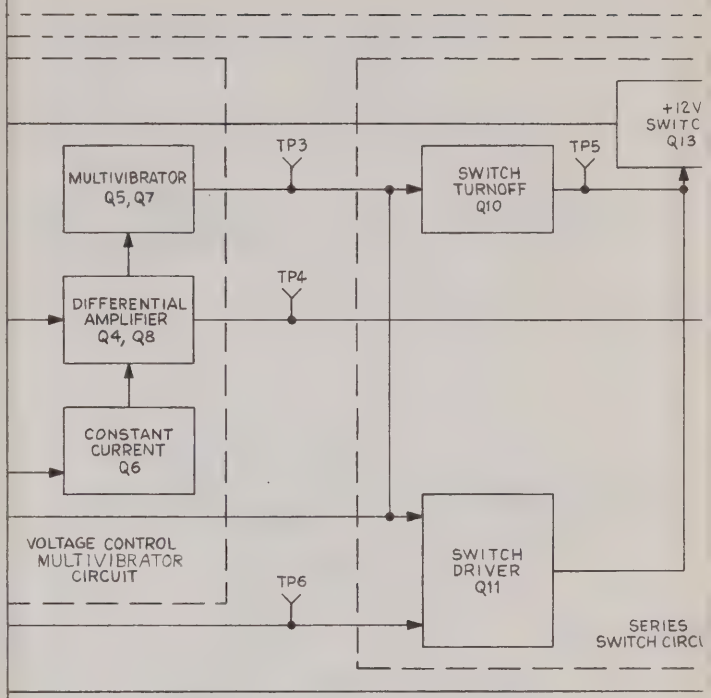
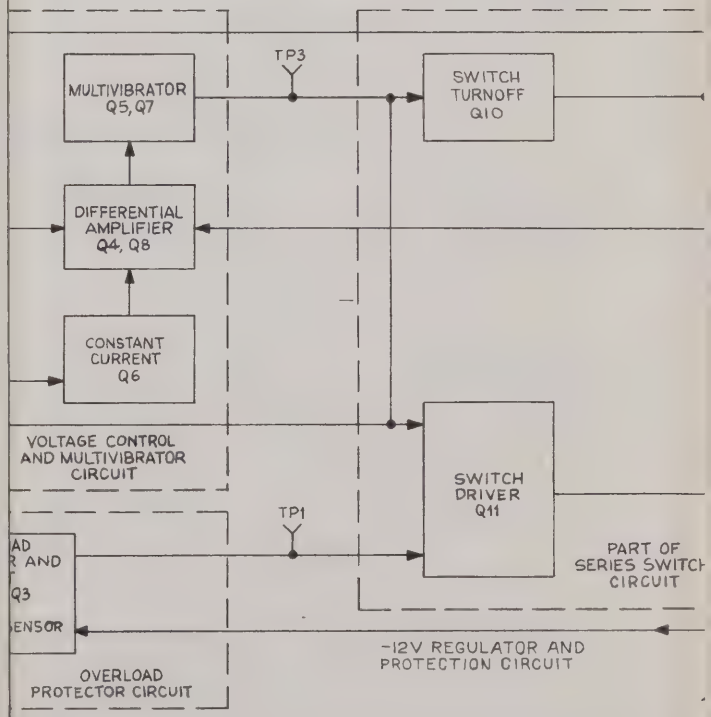


Figure 40. Transmitter subfunction, detailed functional block diagram.


+12V
SWITC
Q13
TP3
TP5
MULTIVIBRATOR
Q5, Q7
SWITCH
TURNOFF
Q10
TP4
DIFFERENTIAL
AMPLIFIER
Q4, Q8
CONSTANT
CURRENT
Q6
VOLTAGE CONTROL
MULTIVIBRATOR
CIRCUIT
SWITCH
DRIVER
Q11
TP6
SERIES
SWITCH CIRCU


TP3
MULTIVIBRATOR
Q5, Q7
SWITCH
TURNOFF
Q10
DIFFERENTIAL
AMPLIFIER
Q4, Q8
CONSTANT
CURRENT
Q6
VOLTAGE CONTROL
AND MULTIVIBRATOR
CIRCUIT
SWITCH
DRIVER
Q11
TP1
AD
R AND
Q3
ENSOR
PART OF
SERIES SWITCH
CIRCUIT
-12V REGULATOR AND
PROTECTION CIRCUIT
OVERLOAD
PROTECTOR CIRCUIT

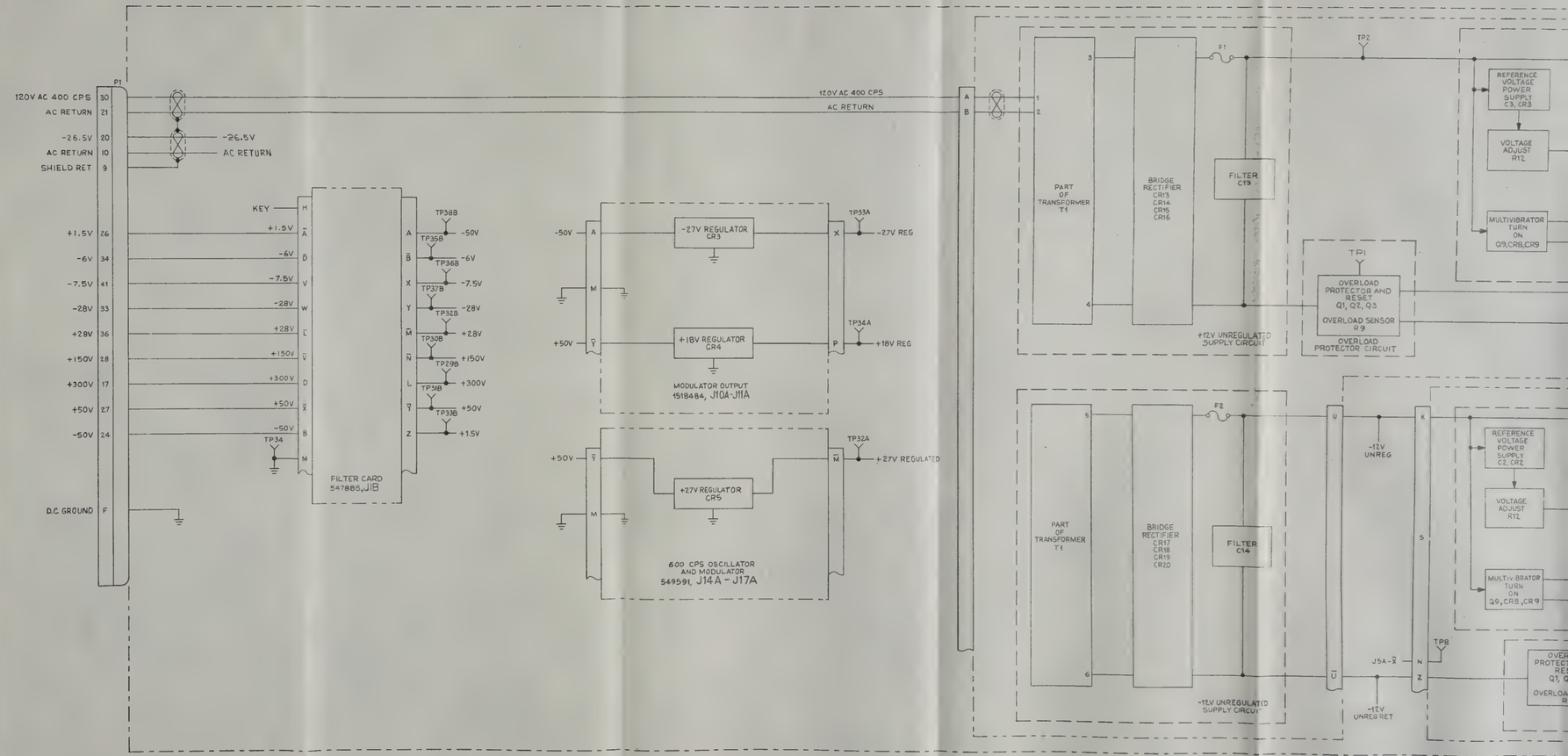


Figure 41. Power supply subfunction, block diagram.

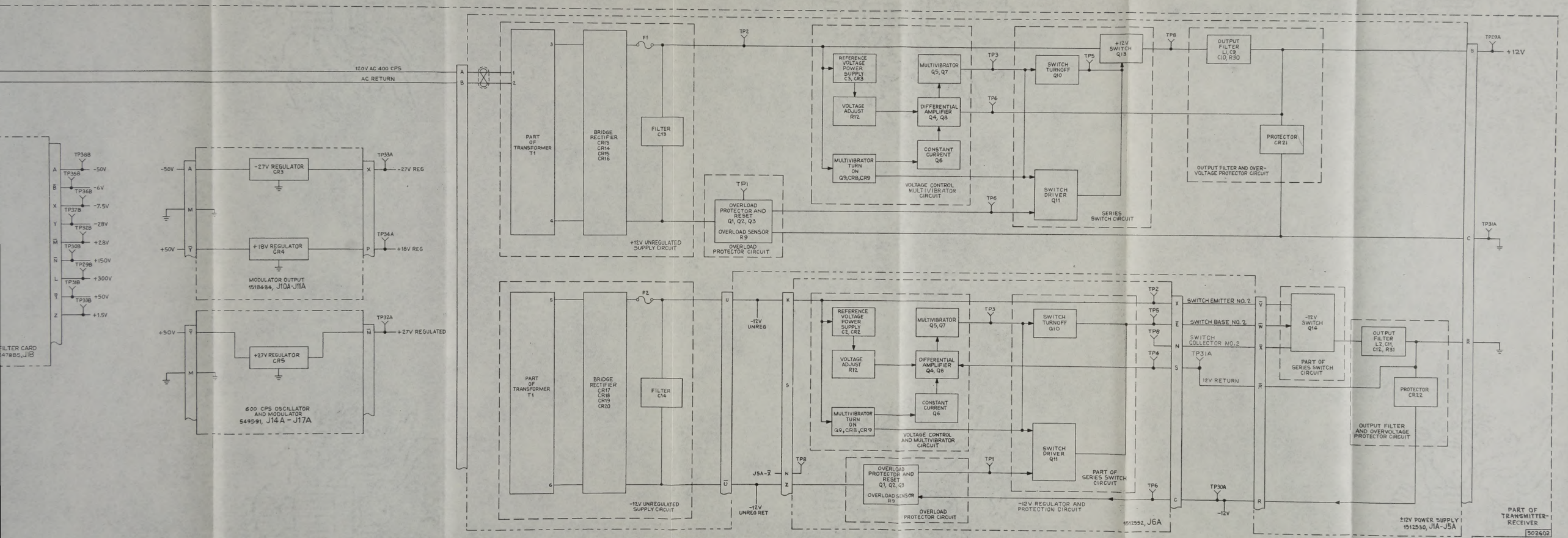
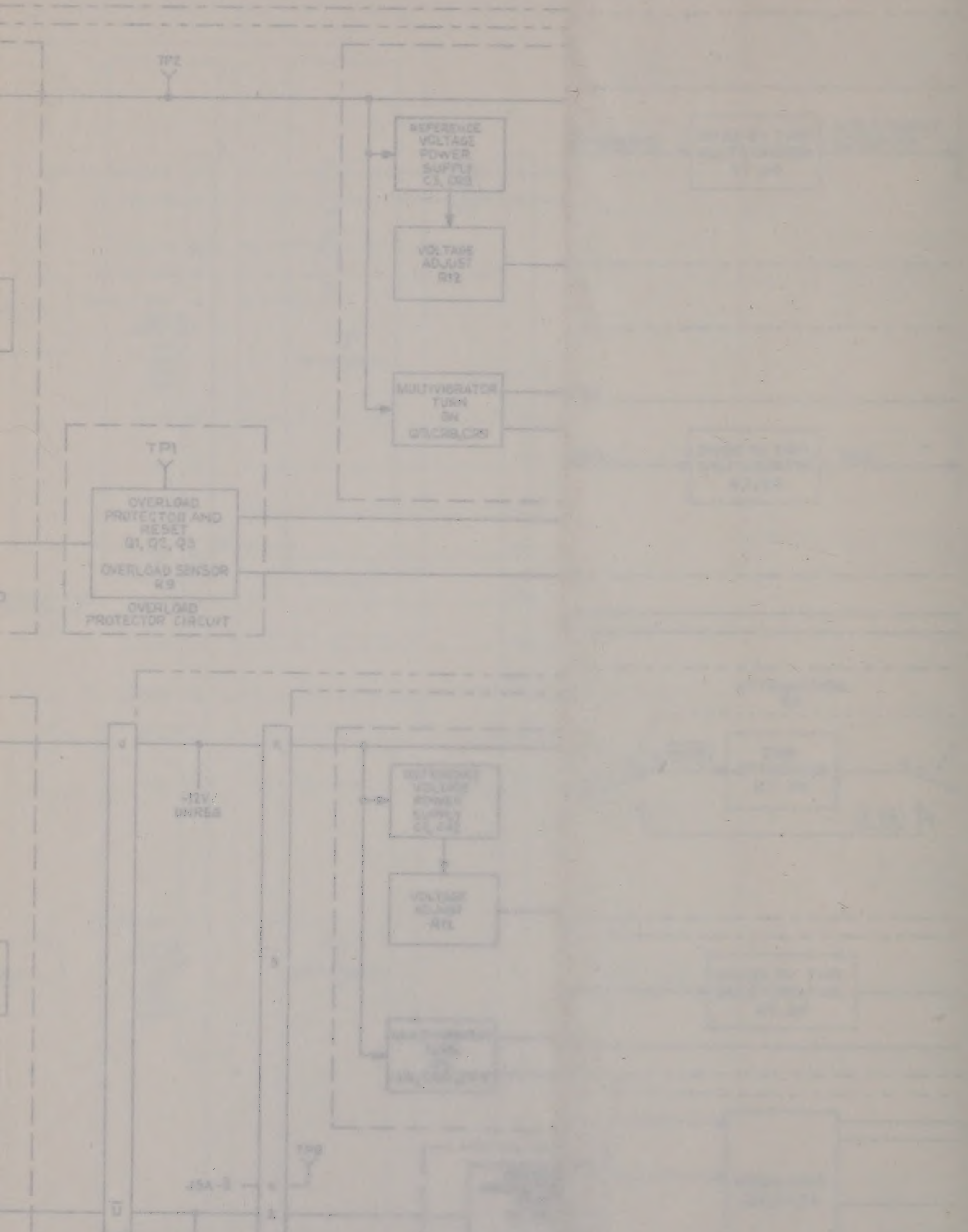


Figure 41. Power supply subfunction, block diagram.



unction, block diagram.